DESIGN OF ON CHIP COPLANAR WAVEGUIDE MATCHING CIRCUIT FOR BI-CMOS RF AMPLIFIER

Haruichi KANAYA, Tetsuya NAKAMURA and Keiji YOSHIDA
Department of Electronics, Graduate School of Information Science and Electrical Engineering, Kyushu University, Fukuoka 812-8581, Japan
Phone: +81-92-642-3954, Fax: +81-92-642-3971
E-mail: kanaya@ed.kyushu-u.ac.jp

Abstract - We studied the new design theory of impedance matching circuits for SiGe BiCMOS low noise amplifier (LNA), power amplifier (PA) and T/R switch for 2.45GHz wireless LAN (IEEE 802.11b) system. Our new matching circuits are composed of conductor-backed coplanar waveguide (CPW) meanderline resonators and impedance inverters. The EM-simulated performances of BiCMOS LNA and PA connected with input and output matching circuits are in agreement with our new design theory.

I Introduction

In the wireless LAN, bluetooth, IMT-2000 and satellite telecommunication systems, RF-CMOS LSI is a key technology in order to make size reduction and cost performance [1]. However, the performance of the CMOS chip has a limitation in the high frequency region, and high-speed application. On the other hand, SiGe bipolar has a higher performance compared to CMOS at relatively low price compared to GaAs device [2].

In the RF section, impedance matching circuit is necessary for interconnecting low noise amplifier (LNA), power amplifier (PA), mixer, and switch. Although the lumped element circuits such as the spiral inductor and MIM capacitor are adopted for matching circuit, it cannot be used at high frequency range because of the self-resonance and stray impedances. On the other hand, distributed elements made of transmission lines are particularly effective because their size becomes smaller, as the frequency is higher.

Moreover, coplanar waveguide (CPW) is easy to fabricate on the CMOS chip because the signal line and ground plane exist only on the same side, and also easy to realize desired characteristic impedance.

In our previous papers [3,4], we proposed a new design method of the broadband impedance matching circuit for interconnecting the on-chip devices such as small antenna, CMOS LNA and PA. In this paper, we designed single chip SiGe BiCMOS RF amplifiers composed of LNA, PA and T/R switch with CPW input and output matching circuits.

II. Design of BiCMOS Amplifiers

Fig.1 shows the block diagram of single chip Tx and Rx amplifiers, which is composed of diode switch, LNA and PA with input and output matching circuits. The designed input and output impedances are 50Ω. The microwave characteristics are simulated by the circuit simulator ADS (Agilent technologies). Fig. 2 and Fig. 3 show the circuit model and layout of the LNA and PA, respectively. The target of the *Max gain* and noise figure (*NF*) of the LNA are 15dB and 2dB at 2.45GHz, respectively. V_{CC} of this process is 3.0V. The circuit parameters, such as spiral inductor and MIM capacitors of the TSMC 035μm BiCMOS process are imported into these simulations. In order to suppress the *NF*, we connect the spiral inductor to the emitter (See Fig. 2). Fig. 4 (a) shows the *NF* circle and gain circle of the LNA without spiral inductor, and Fig.4 (b) shows those of the LNA with spiral inductor at 2.45GHz. The point of the *Max gain* closes to that of the minimum *NF* (NF_{min}) by connecting the spiral inductor. This LNA has *Max gain* = 16.5[dB] and *NF*=1.7[dB]. The *Max gain* of PA is 19.0 [dB].

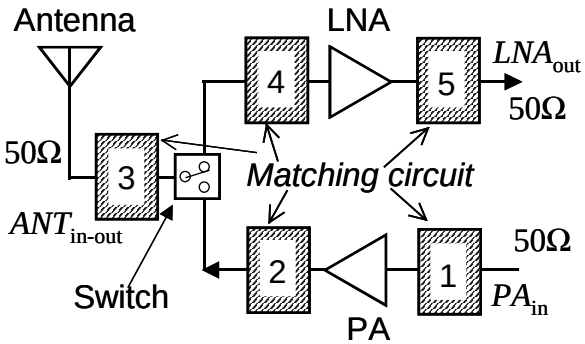

Fig.1. Brock diagram of single chip Tx and Rx amplifiers.

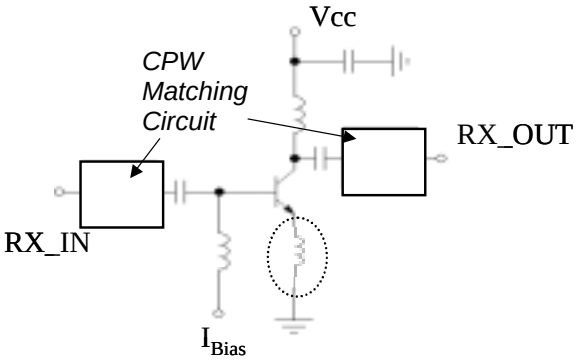

Fig.2. Circuit model of the LNA.

The simulated input and output impedances of PA and LNA are shown in Table 1. We can see those impedances are far from 50Ω.

Fig. 5 and Fig. 6 show the circuit model of the T/R switch and the RF characteristics of this switch, respectively. The insertion Loss is 1.6dB and isolation is 25dB, which is satisfied with the target value. The impedance of the on-state of the this switch is 45.7-*j*2.59[Ω], which is closed to 50Ω, so we can omit the matching circuit #3 (see Fig.1).

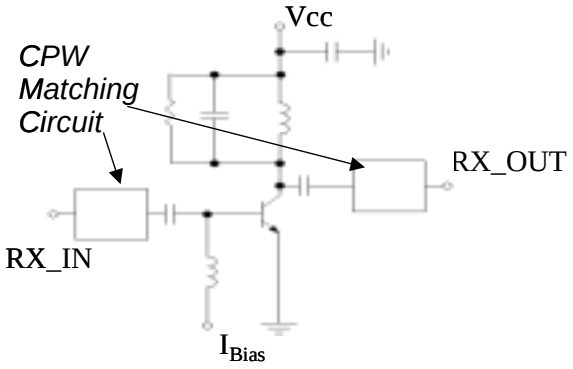

Fig.3. Circuit model of the PA.

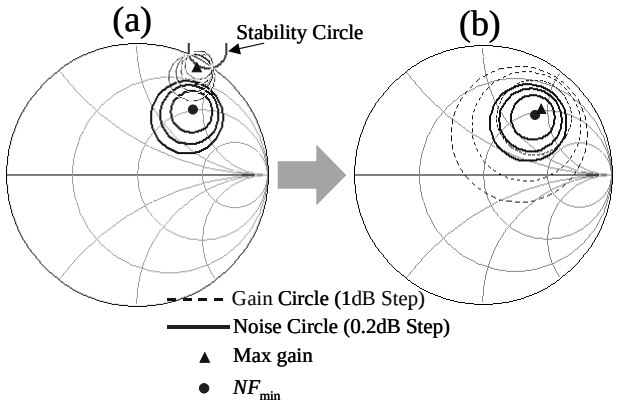

Fig.4. *NF* circle and gain circle of the LNA without spiral inductor (a), and with spiral inductor (b) at 2.45GHz.

TABLE I
Input and output impedances of amplifiers

	Z_{in} [Ω]	Z_{out} [Ω]
PA	1.72–*j*10.2	13.1-*j*21.8
LNA	124–*j*20.4	80.3-*j*32.6

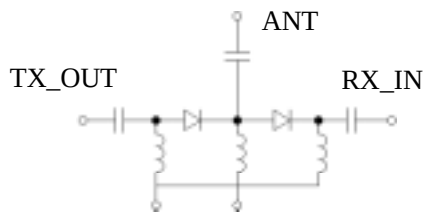

Fig.5. Circuit model of the T/R switch.

Fig.7 shows the circuit model of the quarter wavelength matching circuit. In the figure, Y_L (=G_L+jB_L) is the input admittance of the amplifier. Z_1 and θ are the characteristic impedance and electrical length of the quarter wavelength line, respectively. In order to compensate the jB_L, we adjust the length by $\Delta\ell$ as,

$$\Delta\ell = -\frac{B_L}{\omega_0 C} \quad , \tag{1}$$

where, C is the capacitance per unit length of the transmission line. Finally, *K*-inverter and Z_1 are given by,

$$K_{0,1} = \sqrt{w}\sqrt{\frac{Z_0 x_1}{g_0 g_1}}, \quad \left(x_1 = \frac{\pi}{4} Z_1\right), \tag{2}$$

$$Z_1 = \frac{\pi}{4}\frac{w}{g_1 g_2 G_L}, \tag{3}$$

where, w and g_i are the normalized bandwidth and normalized filter element, respectively [3,4]. The reactance (X_1) and the reactance slope parameter (x_1) are for the series resonance circuit [5]. In the case of noise matching, it is easy to replace Y_L with Y^*_{opt}, where Y_{opt} = G_{opt}+jB_{opt} is the admittance which minimize the noise figure, and given by,

$$\Delta\ell = \frac{B_{opt}}{\omega_0 C} \quad . \tag{4}$$

For size reduction, the quarter wavelength CPW transmission line is bended into meander structure and the CPW meander short stub realizes *K*-inverter.

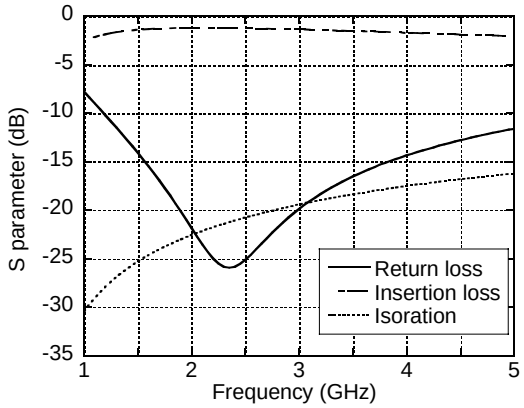

Fig.6. RF characteristics of the T/R switch.

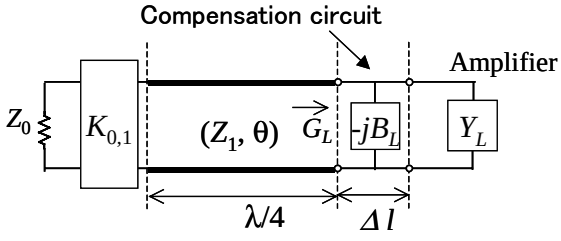

Fig.7. Circuit model of the quarter wavelength matching circuit.

III. Experimental Results of CPW Section

We use the 0.35μm BiCMOS process, which has 1P3M structure. Coplanar waveguide (CPW) matching circuits are designed and simulated by the EM simulator (Momentum, Agilent technologies). In order to avoid the loss in the Si substrate, we covered the lowest metal (metal1) in all area of the CPW structure, namely conductor backed CPW as shown in Fig.8. The conductance of the metal and ε_r of the SiO_2 are 4.1×10^7 S/m and 4.1, respectively. The signal width and the interval between the slots of the transmission line are 8μm and 12μm, respectively. The design parameters of the matching circuit are f_0=2.45GHz and w=100MHz, which is based upon IEEE 802.11b.

Fig.9 shows the image of the CPW matching circuit (a) and photograph of the test chips of the CPW meanderline short stub (*K*-inverter) (b). The CPW measuring PADs are also fabricated on the chip. Fig.10 shows the photograph of the RF measuring system. The microwave characteristics are measured by using air coplanar probe (Cascade Microtech Inc.) and vector network analyzer (HP-8722; HP).

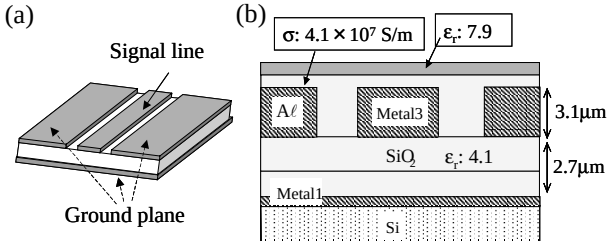

Fig.8. Schematic diagram of the conductor backed CPW (a) and sectional view of the EM-simulated condition (b).

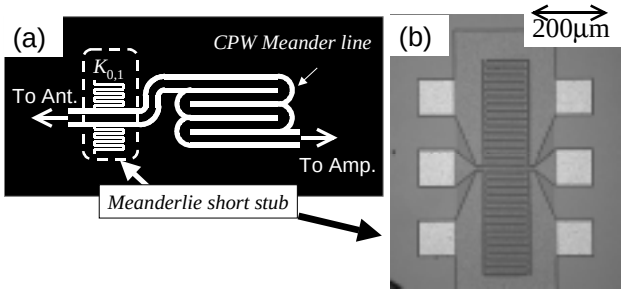

Fig.9. Image of the CPW matching circuit (a) and photograph of the test chips of the CPW meanderline short stub (*K*-inverter) (b).

Fig.11 shows the frequency characteristics of the test chip of the *K*-inverter. In the figure, EM-simulated results are also plotted. EM-simulated data are almost similar to those of the experimental results. The slight difference between the simulation and experimental results are cause of the contact loss between the PAD and the probe. The RF calibration using on chip calibration patterns will reduce this effect. However, it is obvious that we can design the CPW matching circuit by using EM simulator.

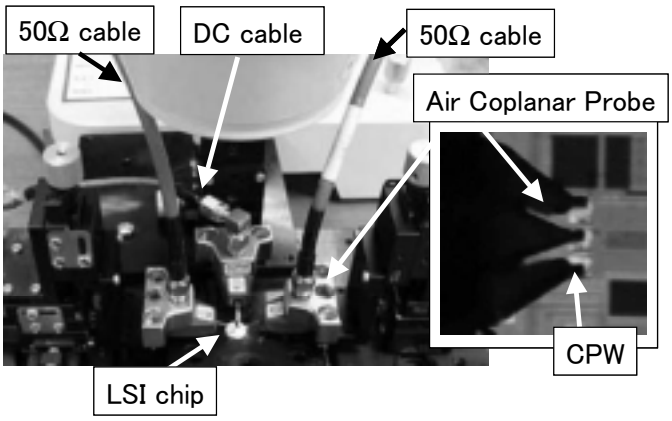

Fig.10. Photograph of the RF measuring system.

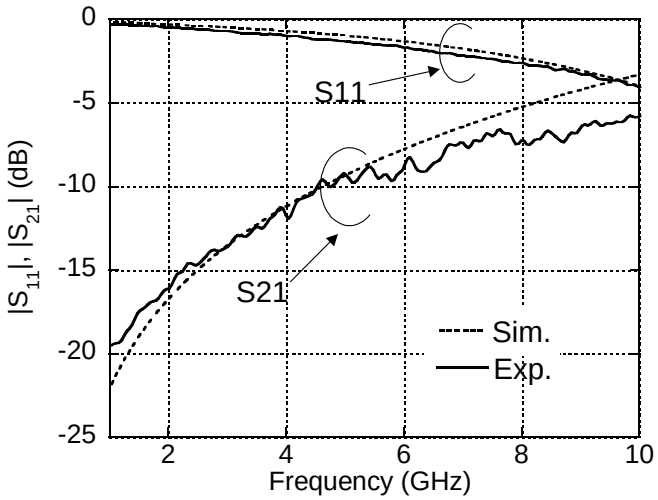

Fig.11. Frequency characteristics of the CPW *K*-inverter.

IV. Layout of Single Chip SiGe BiCMOS Tx and Rx Amplifiers

Fig. 12 shows the layout of the trial chip of the single chip amplifiers with switch. These input and output matching circuits of the PA and LNA have 50Ω-matching at f_0=2.45GHz and w=100MHz (IEEE 802.11b). In order to attach this to the fixed aria in the package, the chip size is 5mm×1.5mm in this case. However, it is easy for more size reduction by reforming the CPW meander structures.

Fig. 13 shows the EM simulated results of the Tx, namely frequency characteristics form PA_{in} to $ANT_{in\text{-}out}$ (see Fig.1). In this time, we shot off the power supply of the Rx section. In this figure, frequency dependence of the isolation (form PA_{in} to LNA_{out}) is also plotted. Fig. 14 shows those of the Rx, namely from $ANT_{in\text{-}out}$ to LNA_{out}. We can see that the gains (S_{21}) of both amplifiers reach the maximum values at around 2.45GHz. The power gain of PA and LNA are

19dB and 15dB, respectively. Both amplifiers have less than 20dB-matching at 2.45GHz. Also we obtain the isolation less than 30dB.

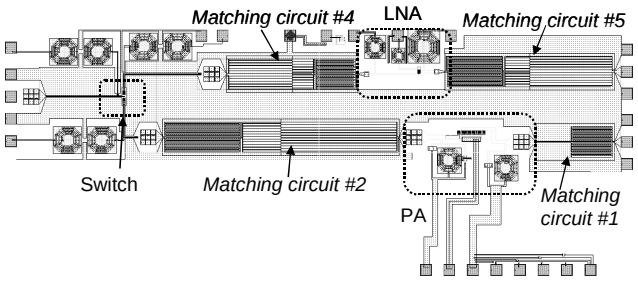

Fig.12. Chip layout of the single chip SiGe BiCMOS Tx and Rx amplifiers (5mm×1.5mm).

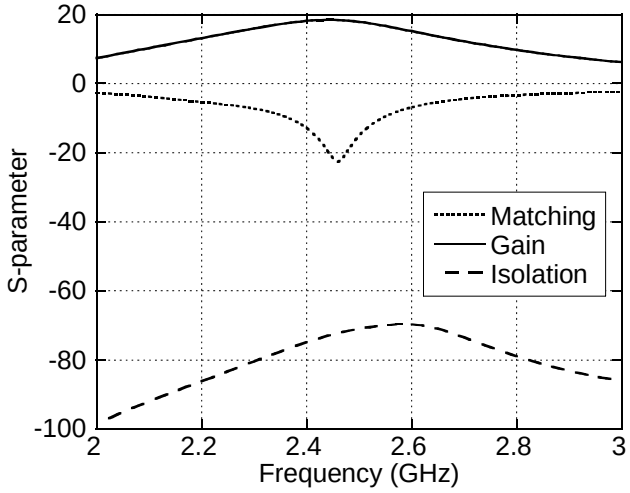

Fig.13. Simulation results of the PA.

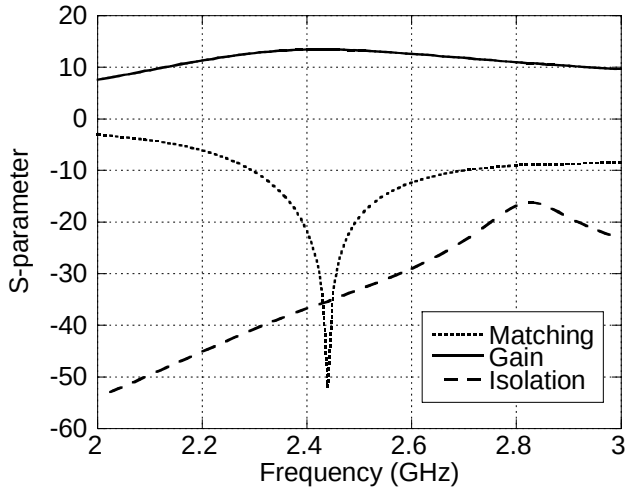

Fig.14. Simulation results of the LNA.

V. Conclusion

We designed the single chip SiGe BiCMOS Tx and Rx amplifiers with matching circuits, which are composed of quarter-wavelength resonators and *K*-inverters. Our new transmission-line-based matching circuit can be designed not only matching but also the bandwidth, which is superior to the lumped element matching circuit. When we design the PA and LNA, the main target is not only to be obtain maximum gain, but also maximum efficiency, minimum distortion, minimum noise figure, and so on, which depend on application specification. These optimum matching conditions are also realized by using this design method instead of the 50Ω matching. Moreover, we can adjust the meander-line shape in order to fit the vacant place on the substrate. We will evaluate the microwave characteristics of the trial chip.

Acknowledgements

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