High temperature superconducting slot array antenna connected with low noise amplifier

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Abstract. For a single chip HTS integrated microwave receiver, a superconducting slot antenna and a SiGe BiCMOS low noise amplifier (LNA) combined with a broad band matching circuit composed of coplanar waveguide (CPW) meanderline resonators has been designed and tested. By applying the filter technique and using inverters, we propose a new design method of CPW broadband impedance matching circuit connected to low or high impedance loads such as HTS antenna or BiCMOS device. For slot antenna, in order to increase the directivity of the antenna, we designed 2-dimensional array antenna by folding the slot antenna. We fabricated and tested YBCO slot array antenna with 3-pole matching circuit by using our present design theory at cryogenic temperature. The prototype YBCO slot array antenna has in good agreement with the simulated results.

1. Introduction

There are many location-free data translations, such as wireless LAN, bluetooth, IMT-2000 and satellite telecommunications. In order to make size reduction and cost performance, there are great expectations of a single chip MMIC, which is composed of low noise amplifier (LNA), power amplifier (PA), mixer, and so on [1]. Moreover, SiGe BiCMOS has better-cost performance than GaAs device. So we applied the SiGe CMOS to RF active device. For suppress the connection loss, impedance matching circuit is necessary for interconnecting above devices. Although the lumped element circuits such as the spiral inductor and MIM capacitor are adopted for matching circuit [2], it cannot be used at high frequency range because of the self-resonance and stray impedance. On the other hand, distributed elements made of transmission lines are particularly effective because their size becomes smaller, as the frequency is higher. Moreover, coplanar waveguide (CPW) is easy to fabricate on the LSI chip because the signal line and ground plane exist only on the same side, and also easy to realize desired characteristic impedance. As a small antenna, there are many reports about the slot antenna fabricated by the normal metal [3]. In our previous papers, we proposed a new design method of the broadband impedance matching circuit for the small antenna [4-6].

In this paper, we generalize the design method of the on-chip matching circuit connecting with the LNA. The circuit simulator and electromagnetic field simulator studies provide the expected performances of the SiGe BiCMOS LNA with the input and output impedance matching circuit. Finally, the 50Ω matching circuit connects the HTS

small antenna with LNA. The prototype YBCO slot array antenna is also designed and tested in the cryogenic temperature.

2. Design of SiGe BiCMOS low noise amplifier

Fig.1 shows the schematic diagram of the low noise amplifier (LNA). The target frequency is 10GHz for satellite base station. The LNA is fabricated in 0.35μm SiGe BiCMOS process, and VCC is 2.5V. In order to raise the power gain, we choose the 2-stage amplifier. The emitter width and length are 0.8μm and 1.9μm, respectively. The characteristics are simulated by the ADS (Agilent technologies). From the data of input and out put impedance and minimum noise figure, we can design the input and output matching circuits as follows.

Fig.2 (a) shows the circuit model of the transmission line based matching circuit and Fig.2 (b) shows the circuit model at resonant frequency. The quarter wavelength line and impedance inverter (K-inverter) compose the matching circuit. In the figure, Y_L ($=G_L+jB_L$) and Z_1 are the input impedance of the LNA and characteristic impedance of the quarter wavelength line, respectively. In order to compensate the jB_L, we adjust the length by $\Delta\ell$ as,

$$\Delta\ell = -\frac{B_L}{\omega_0 C}, \tag{1}$$

where, C is the capacitance per unit length of the transmission line. Finally, the proposed design values for the K-inverter and Z_1 are given by,

$$K_{0,1} = \sqrt{w}\sqrt{\frac{Z_0 x_1}{g_0 g_1}}, \quad x_1 = \frac{\pi}{4}Z_1, \quad Z_1 = \frac{\pi}{4}\frac{w}{g_1 g_2 G_L}, \tag{2}$$

where, w and g_i are the normalized bandwidth and normalized filter element, respectively. The reactance (X) and the reactance slope parameter (x) are for the series resonance circuit. In the case of noise matching, it is easy to show $Z_L=Z^*$opt in eqs. (1) and (2), where, Z_{opt} is the impedance which minimize the noise figure.

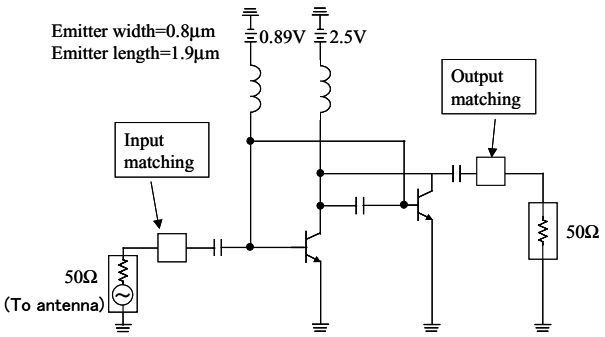

Figure 1. Schematic diagram of the 10GHz 2-stage LNA with input and output matching circuits.

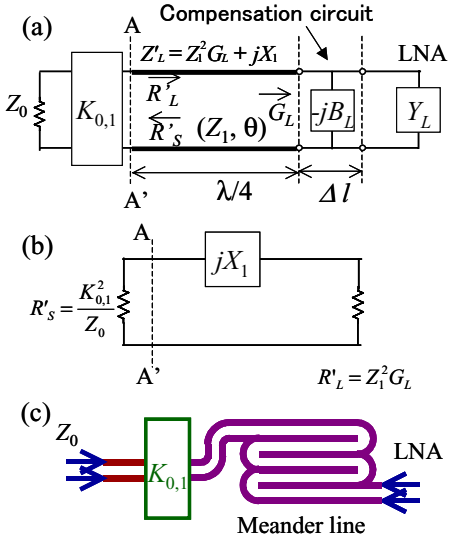

Figure 2. (a) Circuit model of the l/4 matching circuit, (b) equivalent circuit model at resonant frequency and (c) schematic diagram of the CPW matching circuit.

This CMOS chip has a 3-metal layer structure. In order to avoid the loss in the Si, we covered the lowest metal (metal1), namely conductor backed CPW. The conductance of the metal is 4.1×10^7 S/m in this simulation. The signal width and the interval between the slots of the 50Ω line are 5μm and 15μm, respectively. For size reduction, the quarter wavelength line was bended into meander structure (see Fig.2(c)). *K*-inverter is fabricated by using shunt meander inductor. The design parameters of the matching circuit are f_0=10GHz, w=2%. The calculated data of the input and output matching circuits are imported into the circuit model as shown in Fig. 1.

Fig. 3 shows the simulated results of the return loss ($|S_{11}|$) and power gain ($|S_{21}|$) of the LNA with input and output matching circuit. At 10GHz, the power gain and matching property obtain the maximum values. Fig. 4 shows the simulated noise figure (*NF*) of the LNA. In the figure, NF_{min} shows the ideal minimum value that matched the Z_{opt} at all frequency range. Although, *NF* reaches the minimum value at around 10GHz, it dose not minimum because Z_L is slightly different from the Z^*_{opt}. This LNA has gain=11.5dB, *NF*=4.5dB and matching ($|S_{11}|$) =-20dB at 10GHz, respectively. Also we can design the noise matching circuit.

Fig. 5 shows the frequency dependences of the input and output impedance of the LNA. The real part of the input and output impedances are almost equal to the 50Ω at 10GHz. On the other hand, the imaginary part of the input and output impedances are 0Ω. Finally, we will connect the 50Ω feed line of the LNA with HTS slot antenna described in Sec.3 by using flip chip bonding.

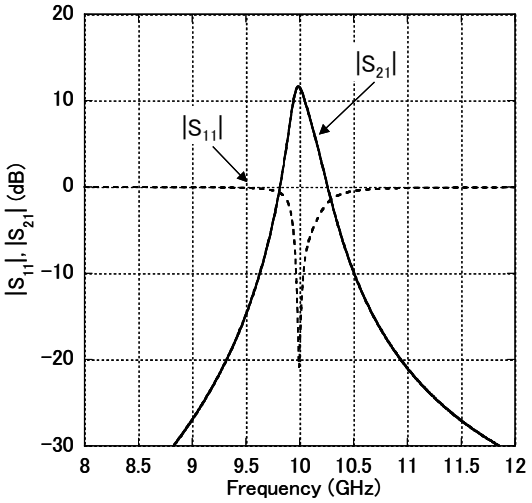

Figure 3. Frequency responses of the insertion loss and return loss of the LNA with matching circuit.

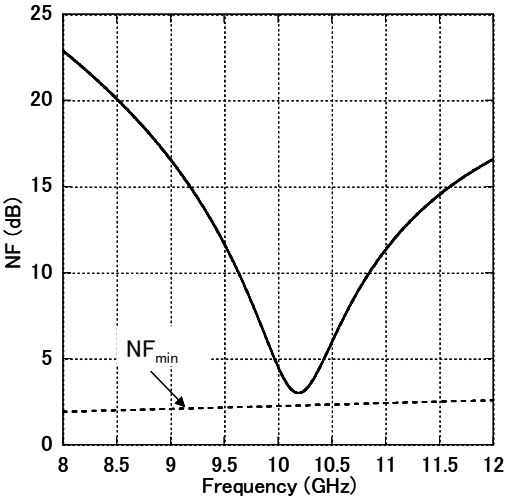

Figure 4. Frequency dependence of the noise figure of the LNA with matching circuit.

3. Design of HTS slot array antenna

In our previous paper, we designed the 1-dimensional HTS slot antenna connected with *n*=3 impedance matching circuit at 10GHz [6]. In this paper, in order to increase the directivity of the antenna, we designed 2-dimensional array antenna by folding the slot antenna and branching out the feed line.

Fig.6 shows the layout of the slot array antenna and definition of the axis for calculating directivity. The value m is a folded number and n is a branched number of the slot array antenna. Since the spatial distribution of the magnitude of the electric field of (m, n)=(1,1) antenna is similar to that of one wavelength magnetic-current dipole antenna, the directivity G_d is given by,

$$G_d(\theta,\phi) = \frac{|\boldsymbol{E}(\theta,\phi)|^2}{\frac{1}{4\pi}\int_0^{2\pi} d\phi \int_0^{\pi} |\boldsymbol{E}(\theta,\phi)|^2 \sin\theta d\theta} \quad , \tag{3}$$

$$\boldsymbol{E}(\theta,\phi) = \frac{\cos(\pi\cos\theta)+1}{\sin\theta} \cdot \frac{\sin[mkd_m \cos\phi \sin\theta/2]}{\sin[kd_m \cos\phi \sin\theta/2]} \cdot \frac{\sin[nkd_n \cos\theta]}{\sin[kd_n \cos\theta]} \quad , \tag{4}$$

where, d_m and d_n is an interval of the dipole antenna and $k=2\pi/\lambda$ [7].

Figure 7 shows the m dependence of the directivity of the slot array antenna at 10GHz, where n=1. For EM-simulation, folding number corresponds to m value, and the directivity is similar to the data calculated as eqs. (3) and (4).

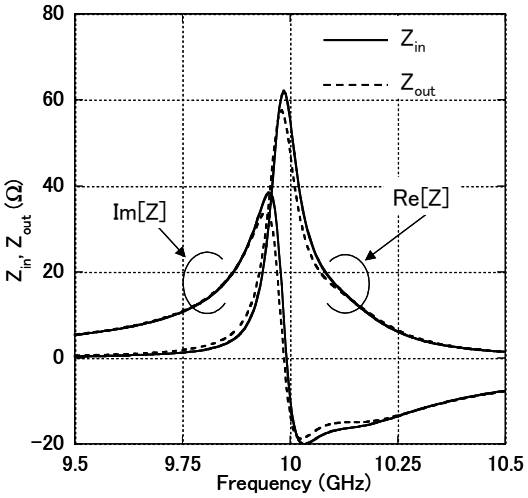

Figure 5. Input and output impedance of the LNA with matching circuit.

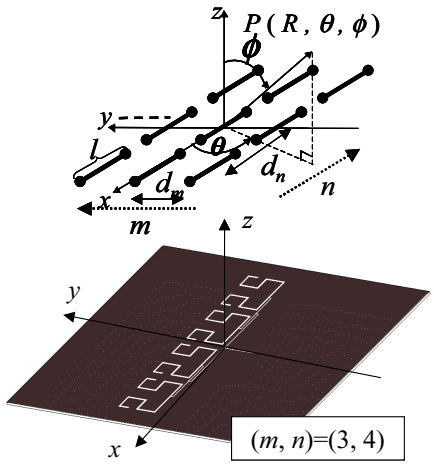

Figure 6. Definition of the axis for calculating the directivity of the slot array antenna.

4. Experimental result of the prototype YBCO slot array antenna

Figure 8 shows the photograph of the prototype YBCO slot array antenna (m, n)=(3, 1) connecting with 50Ω matching circuit. In the figure, the interdigital gaps and meanderline resonators are also printed. The slot width of this slot array antenna is 300μm, so that, radiation resistance (R_a) is 22.88 Ω. We can see the over etching portions in the interdigital gap. We measured S-parameter by using vector network analyzer (HP8722C; HP) though coplanar waveguide probes.

Figure 9 shows the frequency responses of the (m, n)=(3, 1) YBCO slot array antenna with matching circuit at 44K. In the figure, the EM simulation results are also plotted. The

values obtained in this measurement include the residual loss due to the contact between the YBCO film and the metal probe. The center frequency is slightly sifted to the lower frequency because of the kinetic inductance of the YBCO, so that observed data is plotted by the normalized frequency [8]. The observed fractional bandwidth is similar to that of the simulation results. However, because of the over-etching and the residual loss from the connection of the probe, pole frequencies and the base line are not in full agreement with simulation results. We can verify our new design theory by cryogenic experiment.

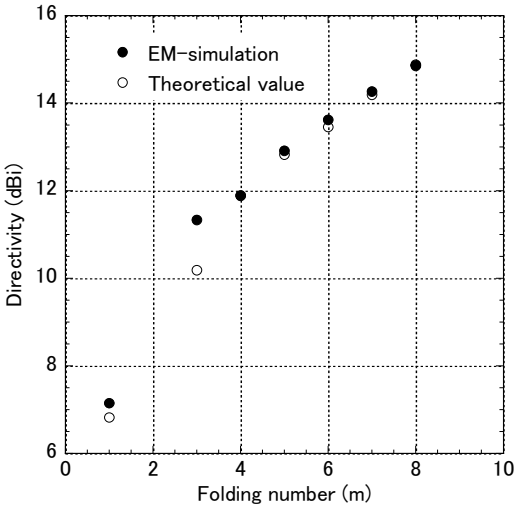

Figure 7. *m* dependence of the directivity of the slot array antenna (*n*=1, at 10GHz).

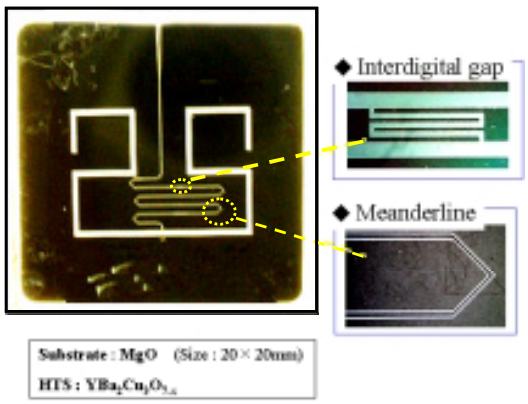

Figure 8. Photograph of the YBCO slot array antenna (*m, n*)=(3,1).

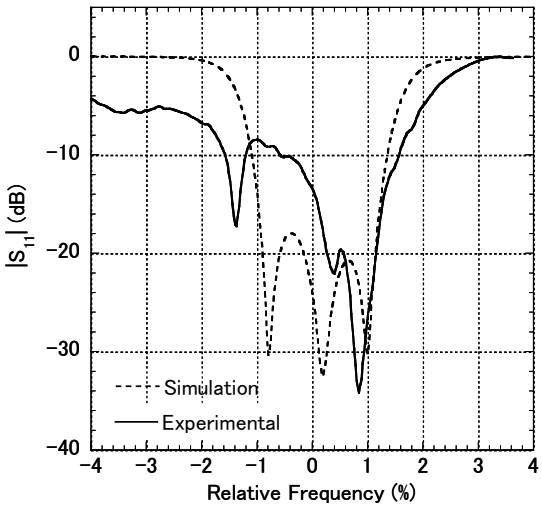

Figure 9. Experimental result of the YBCO slot array antenna at 44K.

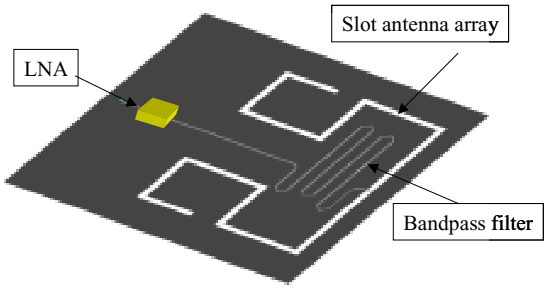

Figure 10. Schematic diagram of the HTS RF receiver.

5. Conclusion

HTS slot array antenna and a SiGe-BiCMOS LNA combined with a broadband matching circuit composed of CPW meanderline resonators has been designed and tested. This broadband impedance matching circuit connects the low and high impedance loads such as HTS antenna and BiCMOS device. Moreover, in order to increase the directivity, we designed 2-dimensional array antenna by folding the slot antenna. The prototype YBCO slot antenna with matching circuit (f_0=10GHz, w=2% and n=3) is also fabricated and tested in the cryogenic temperature. Finally, we will fabricate the THS RF receiver as shown in Fig. 10.

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