Impedance Matching Circuit for Wireless Transceiver Amplifier Based on Transmission Line Theory

H. Kanaya, F. Koga, K. Seki and K. Yoshida
Department of Electronics, Graduate School of Information Science and Electrical Engineering,
Kyushu University
Fukuoka 812-8581, Japan
kanaya@ed.kyushu-u.ac.jp

***Abstract*—This paper presents a new design theory of impedance matching circuits for single-chip SiGe BiCMOS low noise amplifier (LNA), power amplifier (PA) and T/R switch for 5GHz-band wireless LAN (IEEE 802.11a) system. Our matching circuits are composed of conductor-backed coplanar waveguide (CPW) meanderline resonators, and impedance inverter or admittance inverter. The single-chip wireless LAN transceiver amplifier is designed by using the commercial electromagnetic (EM) and SPICE co-simulator. The prototype amplifiers are fabricated and tested.**

I. INTRODUCTION

RF-LSI is a key technology in order to make size reduction and cost performance for the mobile telecommunication systems [1]. Although the performance of the CMOS chip has a limitation in the high frequency and high-speed applications, SiGe bipolar transistor has a higher frequency performance compared to CMOS at relatively low price compared to GaAs device [2].

In the RF section, impedance matching circuits are necessary for interconnecting low noise amplifier (LNA) and power amplifier (PA). Although the lumped element circuits such as the spiral inductor and MIM capacitor are adopted for matching circuit, it cannot be used at high frequency range because of the self-resonance and stray impedances.

Distributed elements made of transmission lines are particularly effective when their size becomes smaller, as the frequency is higher. Distributed elements using transmission lines have already been implemented in GaAs based monolithic microwave integrated circuit (MMIC). However, it will be necessary to fabricate the on-chip matching circuit based on distributed element, in order to operate the RF-CMOS or RF-BiCOMS LSI in the high frequency region.

This work was partly supported by a Grant-in-Aid for Encouragement of Young Scientists (B) from the Japan Society for the Promotion of Science (JSPS). This work was partly supported by a Fukuoka project in the Cooperative Link of Unique Science and Technology for Economy Revitalization (CLUSTER) of Ministry of Education, Culture, Sports, Science and Technology (MEXT).

Among various transmission lines, coplanar waveguide (CPW) transmission line is easy to fabricate on the LSI chip because the signal line and ground plane exist only on the same side. In our previous papers [3,4], we proposed a new design method of the CPW impedance matching circuit for interconnecting the on-chip devices such as small antenna, CMOS LNA and PA.

In this paper, we designed the CPW impedance matching circuits for single-chip SiGe BiCMOS LNA, PA and T/R switch for 5 GHz-band wireless LAN (IEEE 802.11a) systems, by using a commercial electromagnetic (EM) and SPICE co-simulator. (ADS2004A; Agilent Technologies).

II. DESIGN OF 5GHZ AMPLIFIERS

Fig. 1 shows the block diagram of single chip transmitter (*T*x) and receiver (*R*x) amplifiers, which is composed of diode switch, LNA and PA with input and output matching circuits. The designed input and output impedances are 50Ω for general purpose.

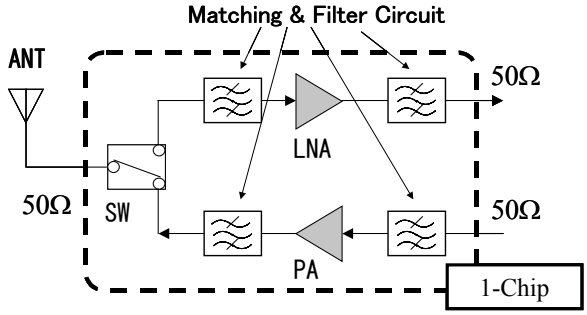

Figure 1. Brock diagram of single chip Tx and Rx amplifier.

Fig. 2 shows the circuit model of the LNA. The PA is the same circuit as that of the LNA, but the size of the

transistors is different. The target of the Max gain of the LNA and PA are 15 dB and 20 dB at 5.2 GHz, respectively. V_{CC} of this process is 3.0V. The circuit parameters, such as spiral inductor and MIM capacitors of the TSMC 0.35 μm BiCMOS process are imported into these simulations. In the figure, circuit model of the matching circuit composed of CPW transmission line and impedance inverter (*K* inverter) or CPW and admittance inverter (*J* inverter) are also presented.

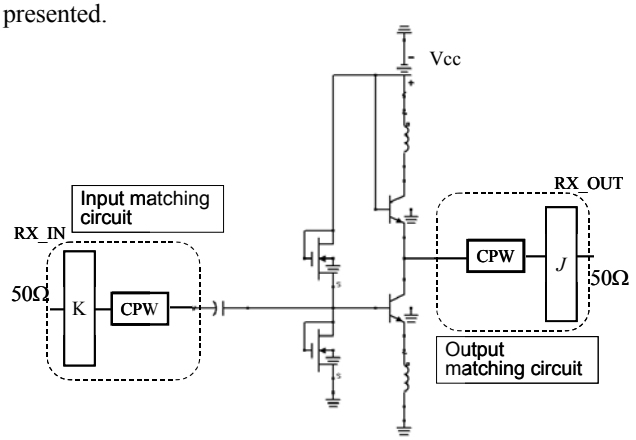

Figure 2. Circuit model of the LNA.

Fig. 3 (a) and (b) show the circuit model of the quarter wavelength matching circuits. Z_1, Y_1 and θ_x are the characteristic impedance, characteristic admittance and electrical length of the quarter wavelength line, respectively.

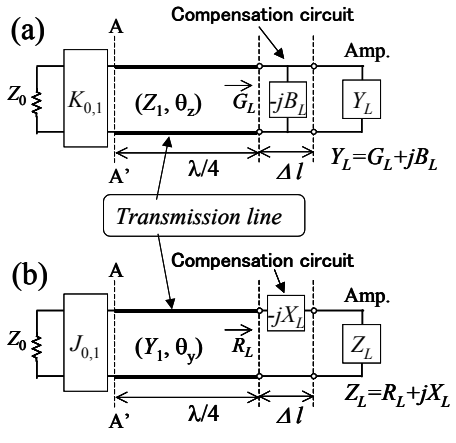

Figure 3. Circuit model of the quarter wavelengh matching circuit of *K* inverter version (a) and *J* inverter virsion (b).

When the input admittance of the amplifier ($Y_L = G_L + jB_L$) is smaller than $1/Z_0$ (=1/50Ω), the design parameters are given by,

$$\begin{cases} \Delta\ell = -\dfrac{B_L}{\omega_0 C} \\ Z_1 = \dfrac{\pi}{4}\dfrac{w}{g_1 g_2 G_L} \\ K_{0,1} = \sqrt{w}\sqrt{\dfrac{Z_0 x_1}{g_0 g_1}}, \quad \left(x_1 = \dfrac{\pi}{4} Z_1\right) \end{cases}, \qquad (1)$$

where, C is the capacitance per unit length of the transmission line, and w and g_i are the normalized bandwidth and normalized filter element, respectively. $\Delta\ell$ is the line length in order to compensate the jB_L. The reactance (X_1) and the reactance slope parameter (x_1) are for the series resonance circuit [5].

On the other hand, when the input impedance of the amplifier ($Z_L = R_L + jX_L$) is smaller than Z_0, the design parameters are also given by,

$$\begin{cases} \Delta\ell = -\dfrac{X_L}{\omega_0 L} \\ Y_1 = \dfrac{1}{Z_1} = \dfrac{\pi}{4}\dfrac{w}{g_1 g_2 R_L} \\ J_{0,1} = \sqrt{w}\sqrt{\dfrac{Y_0 b_1}{g_0 g_1}}, \quad \left(b_1 = \dfrac{\pi}{4} Y_1\right) \end{cases}, \qquad (2)$$

where, L is the inductance per unit length of the transmission line, and w and g_i are the normalized bandwidth and normalized filter element, respectively. $\Delta\ell$ is the line length in order to compensate the jX_L. The susceptance (Y_1) and the reactance slope parameter (b_1) are for the shunt resonance circuit.

III. Experimental Results of The Distributed Elements

Fig. 4 shows the EM-simulation condition and chip photo of the CPW transmission line using a foundry (TSMC Mixed Signal). We use the 0.35 μm BiCMOS process, which has 1-poly 3-metal structure. CPW matching circuits are designed and simulated by the EM simulator (Momentum, Agilent technologies). In order to avoid the loss in the Si substrate, we covered the lowest metal (metal1) in all area of the CPW structure, namely conductor backed CPW. The conductance of the metal is 4.1×10^7 S/m. The signal width and the interval between the slots of the CPW transmission line are 5 μm and 15 μm, respectively. For size reduction, the quarter wavelength line was bended into meander structure.

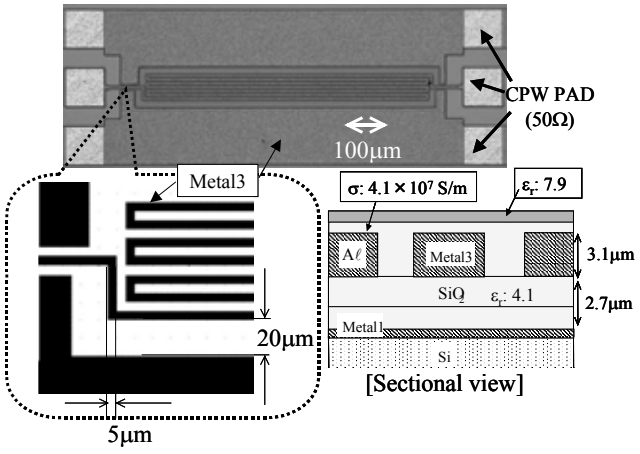

Figure 4. Chip photo of the CPW transmission line and sectional view of the EM-simulated condition.

K inverter and *J* inverter are fabricated by using shunt meander structure and interdigital gap, respectively. Fig. 5 shows the chip photo of the *K* inverter. The input and output microwave characteristics are measured by using air coplanar probes (GSG 150; Cascade Microtech Inc.) and computed controlled vector network analyzer (HP-8722; HP).

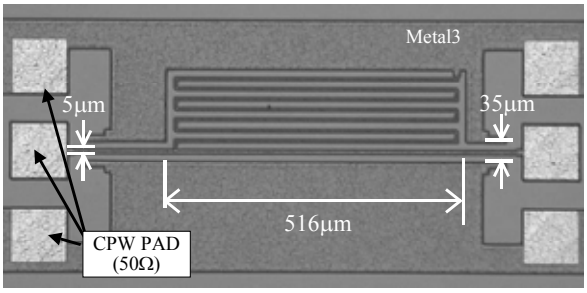

Figure 5. Chip photo of the *K* inverter.

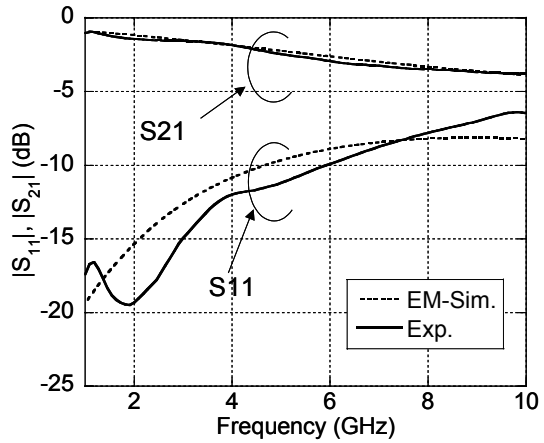

Figure 6. Frequency responses of the CPW meanderline.

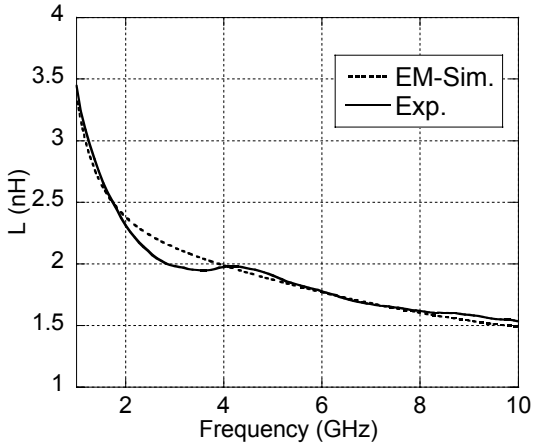

Figure 7. Frequency dependence of the inductance (*L*) of the *K* inverter

Fig. 6 shows the frequency responses of the meanderline CPW transmission line. In the figure, simulated results are also plotted. Insertion loss (S_{21}) of the EM-simulated result is almost in agreement with that of the experimental result. Fig. 7 show the frequency dependence of the inductance (*L*) of the *K* inverter, calculated from the impedance matrix. Experimental value is almost in agreement with that of the EM-simulation result. From Figs. 6 and 7, we can design the distributed circuits by using the EM-simulator.

IV. Simulation and Experimental Results of The Amplifier

The design parameters of the matching circuit are f_0=5.2 GHz and w=100 MHz, which is based upon IEEE 802.11a. Fig. 8 and Fig. 9 show the power gain and return loss of this LNA and PA, respectively. The max gain of the LNA and PA are 21.9 dB and 12.1 dB at around 5.2 GHz, respectively. The current consumption of the LNA and PA are 9.80 mA and 59.1 mA, respectively. We can see that the return loss (S_{11}) of both amplifiers reach the minimum values at around 5.2 GHz, namely, we can design the matching circuit by using CPW transmission line and inverter.

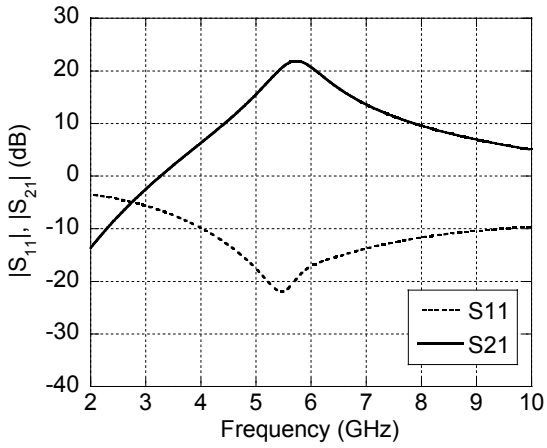

Figure 8. Simulation results of the power gain (S21) and return loss (S11) of the LNA.

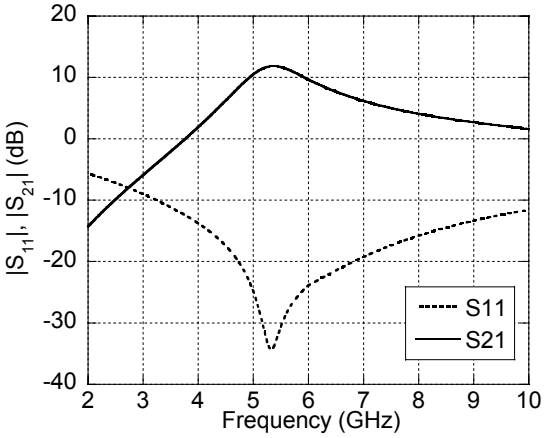

Figure 9. Simulation results of the power gain (S21) and return loss (S11) of the PA.

V. Experimental Results of The Amplifier

Fig 10 shows the chip photo of the single chip SiGe BiCMOS LNA, PA and T/R switch for 5 GHz-band wireless LAN (IEEE 802.11a) systems. The input and output matching circuits are designed by using CPW meander line and *K*- or *J*-inverter respectively. The input and output pads have coplanar configurations those characteristic impedances are 50 Ω. Spiral inductors are used to apply DC power into the transistors. There is a dummy metal in the center of the chip in order to suppress the RF noise. The chip size is 2.2 mm x 1.3 mm. Fig. 11 shows the experimental results of the input impedance of the LNA. In the figure, those of the simulation results are also plotted. The imaginary part of the impedance is similar to that of the simulation result, and the resonance frequency is in agreement with the design value. Because of the effects of the DC feed lines, bonding wires and interconnection among the lumped element circuits such as spiral inductors or MIM capacitors, the real part of the input impedance are 80 Ω instead of 50Ω (design value). However, we can obtain the matching property more than 15 dB in the pass band. The current consumption is 9. 82 mA, which is in agreement with that of the simulation results.

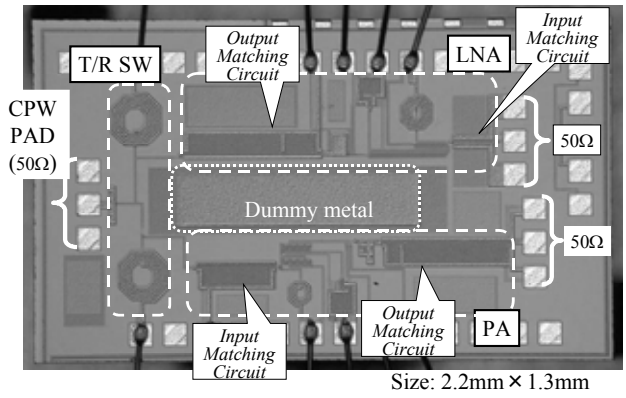

Figure 10. Chip photo of the one chip SiGe BiCMOS Tx and Rx amplifiers

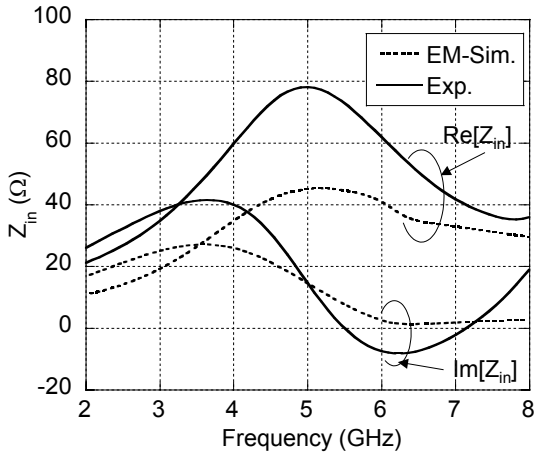

Figure 11. Experimental results of the prototype LNA.

VI. Conclutions

We designed the single chip SiGe BiCMOS Tx and Rx amplifiers with matching circuits, which are composed of quarter-wavelength resonators, and K- or *J*-inverters. When we fabricate the matching circuit for the amplifier, which has high input impedance (for example Z_L=100-*j*1,000Ω at 5GHz), the size of the CPW matching circuit is 30% as small as that composed of spiral inductor. Moreover, our new transmission-line-based matching circuit can be designed not only matching but also the bandwidth, which is superior to the lumped element matching circuit.

When we design the PA and LNA, the main target is not only to obtain maximum gain, but also maximum efficiency, minimum distortion, minimum noise figure, and so on, which depend on application specifications. These optimum matching conditions are also realized by using this design method instead of the 50Ω matching. Moreover, we can adjust the meander-line shape in order to use the vacant place on the substrate effectively.

Acknowledgment

This work was partly supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with CADENCE Corporation. This work was partly in collaboration with Fukuoka Laboratory for Emerging and Enabling Technology of SoC (FLEETS).

References

[1] A. Matsuzawa, "RF-SoC-expectations and required conditions", IEEE. Trans. Microwave Theory Tech., vol. 50, pp. 245-253, 2002

[2] D. L. Harame, et, al., "Currrent status and future trends of SiGe BiCMOS technology," IEEE. Trans. Electron Device, vol. 48, pp. 2575-2594, 2001.

[3] K. Yoshida, T. Takahashi, H. Kanaya, T. Uchiyama, and Z. Wang, "Superconducting slot antenna with broadband impedance matching circuit," IEEE Trans. Appl. Supercond., vol. 11, pp. 103-106, 2001.

[4] H. Kanaya, Y. Koga, J. Fujiyama, G. Urakawa, and K. Yoshida, "Design and performance of high Tc superconducting coplanar waveguide matching circuit for RF-CMOS LNA", IEICE Trans. Electron., vol.E86-C, No.1, pp.37-41, 2003.

[5] H. Kanaya, G. Urakawa, R. Oba and K. Yoshida, "Development of CMOS coplanar waveguide matching circuit for RF front-end", 2003 Asia-Pacific Microwave Conference Proceedings, vol.3, pp.1692-1695, 2003.