High Temperature Superconducting Coplanar Waveguide Matching Circuit for RF Front -End

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Abstract **For realizing a single chip HTS integrated microwave receiver, a superconducting slot antenna and a Si-CMOS low noise amplifier (LNA) combined with a broad band matching circuit composed of coplanar waveguide (CPW) meanderline resonators has been designed and tested. By applying the filter technique and using admittance inverters (*J* inverters), we propose a new design method of CPW broadband impedance matching circuit connected to low and high impedance loads such as HTS antenna and CMOS device. Based on the design method, we designed a Chebyshev type impedance matching circuit connecting with slot antenna and CMOS-LNA.**

Key words: **Broadband impedance matching circuit, HTS slot antenna, CMOS low noise amplifier, Coplanar waveguide**

1. Introduction

With the remarkable demands of location-free data translations, such as wireless LAN, bluetooth, IMT-2000 and satellite telecommunications, there are many investigations of RF devices such as antenna, bandpass filter (BPF) and so on. For active devices, there are great expectations of RF-CMOS devices such as low noise amplifier (LNA) [1]. Moreover, there are many reports on High T_c superconducting (HTS) BPF [2,3] and HTS BPF based cryogenic receiver front-end [4] is being fabricated for commercial use. Figure 1 shows the typical block diagram of wireless terminal and RF section. Impedance matching circuit is necessary for interconnecting above devices. Although the lumped element such as the spiral inductor and MIM capacitor are adopted for matching circuit, it cannot be used at high frequency range because of the self-resonances and stray impedances.

On the other hand, distributed element made of transmission line is particularly effective because its size becomes smaller, as the frequency is higher. Coplanar waveguide (CPW) is easy to connect the CMOS chip because the signal line and ground plane exist on the same side [5].

In our previous paper [6], we proposed a new design method for the broadband impedance matching circuit for the small antenna. In this paper, we generalize the design method to the matching circuit connecting the slot antenna with the CMOS LNA (see Fig. 1). By obtaining the radiation resistance and the antenna reactance, and input impedance of the CMOS LNA for the susceptance slope parameters, we can design the fractional bandwidth and return loss in the passband of the matching circuit. The circuit simulator and electromagnetic field simulator studies provide the expected performances of the slot antenna and CMOS LNA with the impedance matching circuit designed with the present method.

The prototype HTS practical device, which integrates the slot antenna and the CPW 50Ω-matching circuit within 15 mm x 6 mm dimensions on the YBCO film, and its performance was tested in the cryogenic temperature.

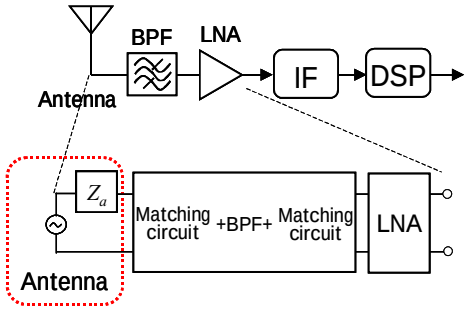

Fig. 1 Block diagram of wireless terminal and RF section.

2. Design Theory of Broadband Impedance Matching Circuit

The present theory is based on the conventional design theory for the *n*-pole BPF [7]. BPF can be realized by using the opened resonators connected with J inverters ($J_{i,\ i+1}$). Figure 2 shows the circuit model of the LNA section, which is assumed to have load impedance (Z_L)=R_L+jX_L.

At first, we propose the method for conjugate matching. In order to make impedance inversion, we insert the quarter wavelength transmission line, which has length (ℓ), electrical length (θ) and characteristic impedance (Z_0) (see Fig. 2(a)). When $|Z_L|>>Z_0$ and ℓ is $\lambda/4$, it can be easily shown that the input impedance Z'_L seen from the left of the transmission line is approximately given by,

$$\left.\begin{aligned} Z'_L &\cong jX' + \frac{Z_0^2}{Z_L} \\ X' &= X + \omega_0 L \Delta\ell \end{aligned}\right\}, \qquad (1)$$

where the reactance (X) and the reactance slope parameter (x) are given by,

$$\left.\begin{aligned} X &= -Z_0 \cot\theta \cong x\left(\frac{\omega}{\omega_0}-\frac{\omega_0}{\omega}\right) \\ x &= \frac{\omega_0}{2}\left.\frac{\partial X}{\partial \omega}\right|_{\omega=\omega_0} = \frac{\pi}{4}Z_0 \end{aligned}\right\} . \qquad (2)$$

Inverted Z_L can be expressed as,

$$\frac{Z_0^2}{Z_L} = \frac{Z_0^2 R_L}{R_L^2+X_L^2} - j\frac{Z_0^2 X_L}{R_L^2+X_L^2} \equiv R'_L + jX'_L \quad . \qquad (3)$$

In order to compensate the jX'_L, we adjust the length by $\Delta\ell$ as (see Fig.2(b)),

$$\Delta\ell = -\frac{X'_L}{\omega_0 L} = \frac{Z_0^2 X_L}{\omega_0 L\left(R_L^2+X_L^2\right)} \quad , \qquad (4)$$

where, L is the inductance per unit length of the transmission line.

In the case of noise matching, it is easy to show $Z_L=Z^*_{\text{opt}}$ ($Z_{\text{opt}}=R_{\text{opt}}+jX_{\text{opt}}$ is the impedance which minimize the noise figure), and $\Delta\ell$ is given by,

$$\Delta\ell = -\frac{Z_0^2 X_{opt}}{\omega_0 L\left(R_{opt}^2+X_{opt}^2\right)} \quad . \qquad (5)$$

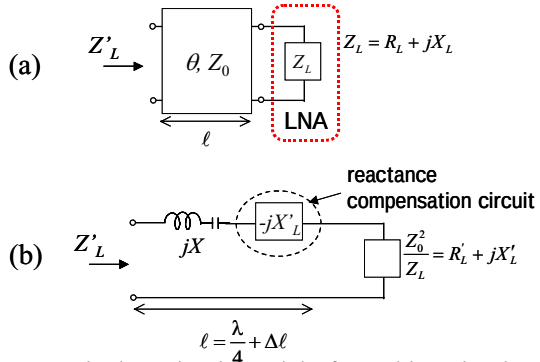

Fig. 2 Equivalent circuit model of matching circuit of LNA section: (a) circuit model and (b) equivalent circuit for $\ell=\lambda/4+\Delta\ell$.

Figure 3 shows the circuit model of n-pole broadband matching circuit connecting with the antenna and LNA, where antenna impedance is $Z_a=R_a+jX_a$. The proposed design values for the admittance inverters (J-inverters) are given by,

$$\left.\begin{aligned} J'_{0,1} &= \sqrt{w}\sqrt{\frac{b'_1}{R_a g_1}} \\ J'_{1,2} &= w\sqrt{\frac{b'_1 b_2}{g_1 g_2}} \\ J_{i-1,i} &= w\sqrt{\frac{b_{i-1}b_i}{g_{i-1}g_i}} \qquad (i=3,4,\cdots,n-1) \end{aligned}\right\} , \qquad (6a)$$

$$\left.\begin{aligned} J'_{n-1,n} &= w\sqrt{\frac{b_{n-1}b'_n}{g_{n-1}g_n}} \\ J'_{n,n+1} &= \sqrt{w}\sqrt{\frac{b'_n}{R'_L g_n}} \end{aligned}\right\} , \qquad (6b)$$

$$\left.\begin{aligned} b'_1 &= \frac{b_1}{1-\frac{wx_a}{R_a g_1}} \\ b'_n &= \frac{b_n}{1-\frac{wx}{R'_L g_n}} \end{aligned}\right\} , \qquad (7)$$

where, x_a is the reactance slope parameter at the series resonance of the antenna impedance (see Ref.[6]), and b_i is the susceptance slop parameter of the $\lambda/2$ resonator which has susceptance B_i. g_i and w are normalized filter elements and fractional bandwidth, respectively. Substituting x of $\lambda/4$ line and R'_L into b'_n, we can design the matching circuit with high impedance element. The b'_1 and b'_n in Eqs. (7) must be positive values. From Eqs. (6), the minimum constriction is n=2, where the total length of the matching circuit is as small as $5\lambda/4$.

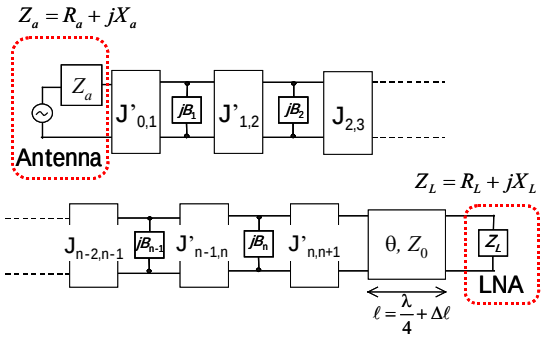

Fig.3 Circuit model of the n-pole matching circuit.

CMOS differential amplifier (gate length and width are 0.6μm and 10μm) was designed and its gain, noise figure and Z_L are simulated by the HSPICE (Avanti!). Figure 4 shows the layout of LNA. We obtained that Z_L of the CMOS LNA is 3.0-j3.3 (kΩ) at 2GHz.

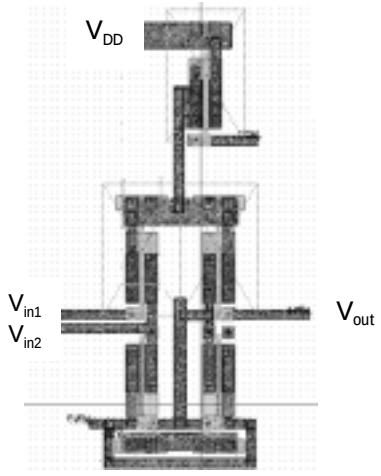

Fig.4 Layout of the differential amplifier.

3. Simulation Results of Broadband Matching Circuit

At first, we discuss the properties of matching circuit connecting LNA with 50Ω line, namely, in the case of Z_a=R_a=Z_0 in Eqs. (6) and (7). So that, $J_{0,1}$ and $J_{1,2}$ are rewritten by,

$$\left.\begin{aligned} J_{0,1} &= \sqrt{w}\sqrt{\frac{b_1}{Z_0 g_1}} \\ J_{1,2} &= w\sqrt{\frac{b_1 b_2}{g_1 g_2}} \end{aligned}\right\} . \qquad (8)$$

The design parameters are f_0=2GHz, w=15MHz and return loss in the passband =20dB. Figure 5 shows the input return losses of the LNA with the n=5, 3 and 1 matching circuit. In the figure, the response of the direct connection of the LNA with the 50Ω line is also plotted. It is shown the bandwidth at 20dB return loss is realized, and skirt characteristic become sharper as n increases.

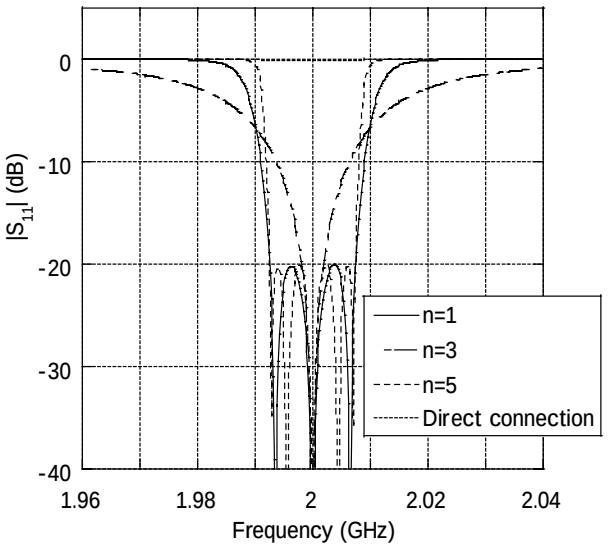

Fig. 5 Input return loss of the LNA with the n -pole matching circuit (f_0=2GHz, w=15MHz and return loss in the passband =20dB).

Figure 6 shows the frequency dependence of the input impedance (Z_{in}) seen from the left of the inverter $J_{0,1}$. R_{in} and X_{in} are almost matched to Z_0 (=50Ω) in the center frequency =2GHz and w=15MHz. These characteristics have Chebyshev ripples in the passband.

Next, the matching circuit is connected the LNA with the slot antenna, instead of 50Ω line (see Fig. 3). Figure 7(a) and (b) show the frequency dependences of the Z_{in} seen from the left of the inverter $J'_{0,1}$, where, R_a=1 Ω and 5Ω, respectiverly. R_{in} and X_{in} are almost matched to R_a in the passband. These characteristics have also Chebyshev ripples.

Figure 8 shows the CPW layout of broadband matching circuit, where, J-inverters are realized by the interdigital gaps. For the size reduction, we adopt the mender line structure for the transmission line. We assume that the lossless conductor is placed on the MgO substrate with thickness on 0.5mm and relative dielectric constant = 9.6, so that, $\Delta\ell$ is calculated as –85.8μm at 2GHz from Eq. 4.

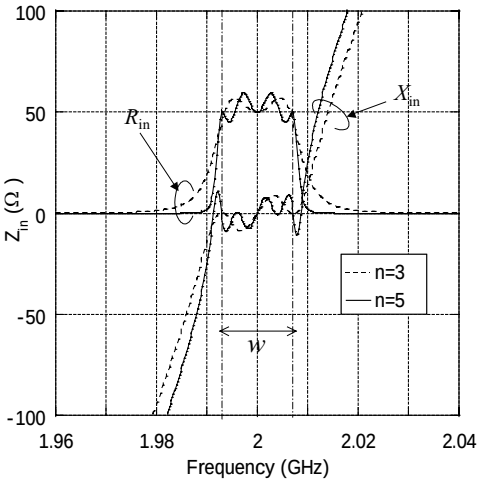

Fig.6 Frequency dependences of the input impedance Z_{in} of the n pole matching circuit (Z_{in} =Z_0).

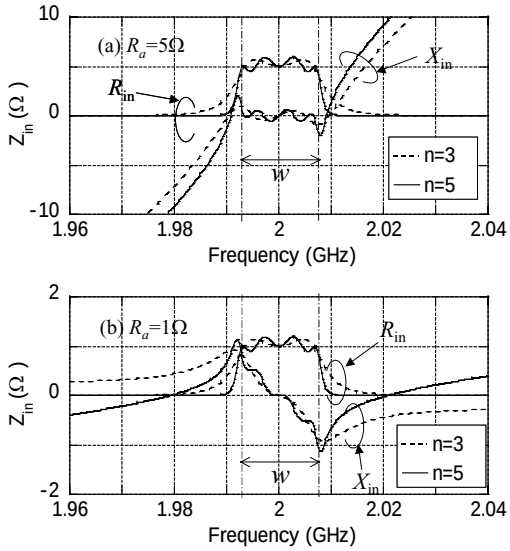

Fig.7 Frequency dependences of the input impedance Z_{in} of the n pole matching circuit (Z_{in} =R_a). (a): R_a=5Ω, (b): R_a=1Ω.

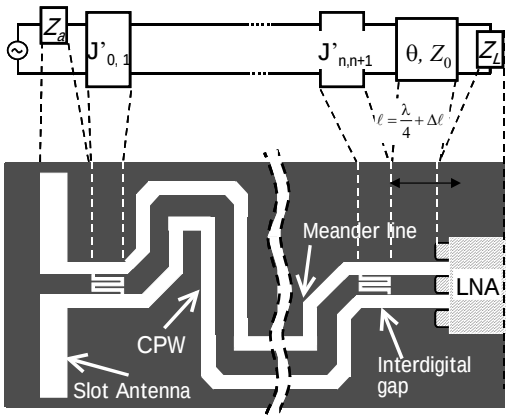

Fig.8 CPW layout of matching circuit of antenna and LNA.

4. Experimental Results of Prototype YBCO CPW Impedance Matching Circuit.

The prototype YBCO CPW impedance matching circuit (n=3) is designed by using EM-simulator (Agilent: Momentum). Because of the restriction of the YBCO film size, we chose the center frequency is 10GHz and w=70MHz. The return loss in the passband is 20dB. Figure 9 shows the photographs of the experimental pattern of the prototype slot antenna with 50Ω-impedance matching circuit. The simulation result of R_a of this slot antenna is 5.0Ω.

Figure 10 shows the frequency responses of the n=3 YBCO matching circuit at 28K. In the figure, simulation results are also plotted. The observed center frequency and fractional bandwidth are similar to that of the simulation results. However, because of the over-etching and the residual loss from the connection of the coplanar probe, pole frequencies and the base line are not in full agreement with simulation results.

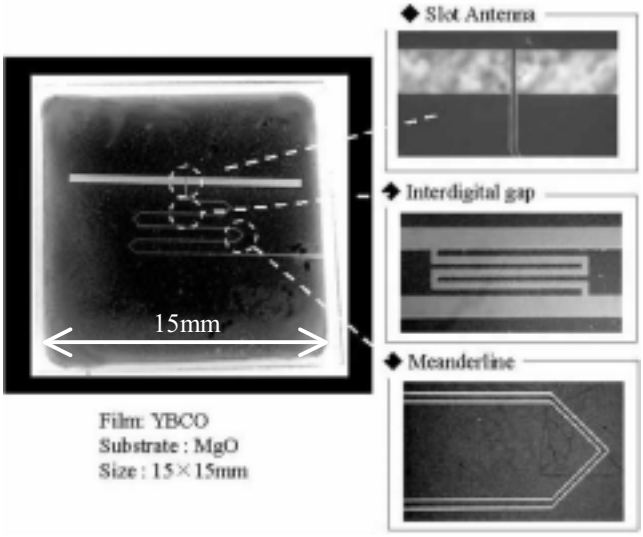

Fig.9 Photographs of the prototype slot antenna with matching circuit.

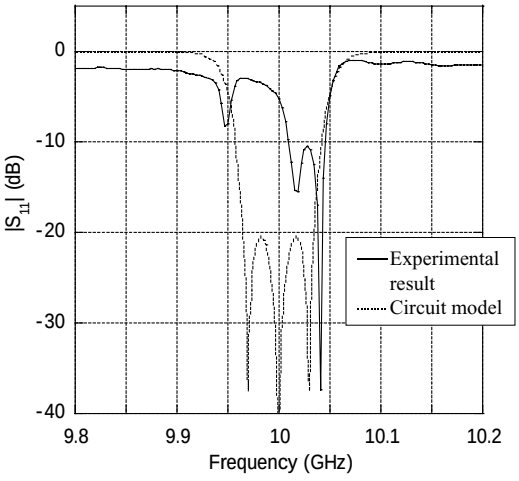

Fig. 10 Experimental results of YBCO slot antenna with n =3 matching circuit at 28K.

5. Conclusions

We present a design theory for the broadband impedance matching circuit connecting the slot antenna with LNA, which incorporates the radiation resistance and the antenna reactance, and input impedance of the CMOS LNA into the susceptance slope parameters of the conventional filter theory. The performance of the prototype HTS practical device, which integrates the slot antenna and the CPW matching circuit, was tested in the cryogenic temperature. Design of the on chip matching circuits for RF-CMOS is also in progress.

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