Design of High-Linearity Amplifier for Wireless LAN Transceiver

O. Nizhnik, R.K. Pokharel, H. Kanaya, and K. Yoshida
Graduate School of Information Sciences and Electrical Engineering
Kyushu University, Fukuoka 819-0395, Japan

Abstract - **High third-order intercept output point (OIP3) RF amplifier, suitable for cheap semiconductor technology is proposed. The circuit functionality simulated using Agilent ADS and parasitic components were taken into account using Assura RCX chip design software. Chip has designed for TSMC 0.35-um BiCMOS process. An OIP3 over +30dBm was achieved with a gain of 8 dB, noise figure 5dB, and a power consumption 80 mW. Amplifier is intended to be used in receiver and transmitter paths of the 802.11a/b/n wireless LAN front-end in 5 GHz band.**

I. Introduction

High-linearity amplifier is designed for the WLAN front-end without PLL. Amplifier is conforms to the specifications of IEEE 802.11a/b/n and HiperLAN standarts.

Intermodulation products, as was shown in [1] may limit the performance of OFDM systems. Up to date there are 3 main approaches to design of high–linearity amplifier. The brief introduction for each approach, their advantages and disadvantages are summarized in Table 1.

TABLE 1. APPROACHES TO REDUCE AMPLIFIER NONLINEARITY

Linearization class	Basic means	Main advantages	Main drawbacks
Analog predistortion [2],[3]	Nonlinear transformation reducing nonlinearity of transfer function	Excellent power efficacy at low frequencies	Degraded NF, limited performance, circuit often complex.
Harmonic termination [4]	Linear filtering by means of filters or frequency-selective amplifier	Does not affect much gain and power consumption	Only narrow bandwidth amplifiers possible
Feedforward [5],[6]	Auxiliary amplifier subtracts IM3 product from output current	Components count is low, sometimes added one transistor	Bad power efficacy, and device dependence

Using only simple memoryless analog predistortion performance improvement is limited [2], if more complex predistortion scheme is used [3], noise figure and bandwidth are significantly degraded.

Basic approach to universal feedforward-linearized amplifier was shown in [5], and so provided 3 basic architectures of linearized amplifier, shown in Fig. 1.

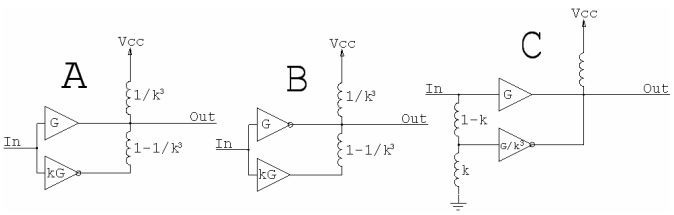

Figure 1. Architectures of feedforward-linearized amplifier. A -feedforward, B - inverting feedforward, C - feedforward with input voltage divider.

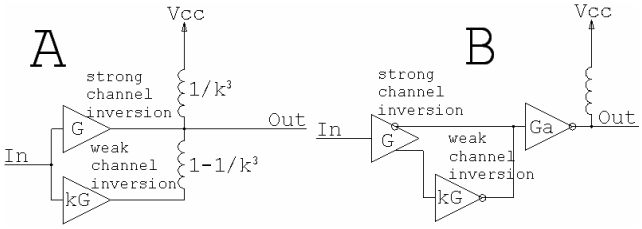

Figure 2. Architectures of MOSFET pair based linearized amplifiers. (A) – improved feedforward amplifier [6], (B) – predistortion/feedforward amplifier [6], [9].

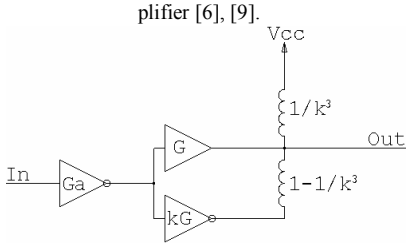

Figure 3. Proposed architecture of universal predistortion/feedforward linearized amplifier. On figure amplifier dominated by 3rd-order distortion.

In Fig. 1 - Fig. 3 voltage gain G is defined as $G = g_m j\omega L_{out}$. Several attempts was made to implement linearized amplifier using transfer characteristic specific for MOS enrichment-mode transistors [6]. These designs are based on fact what nonlinearity components are shifted 180 degrees if transistor channel change from weak inversion mode to strong inversion mode. If weak inversion and strong inversion transistors are included in cascade, it comprises predistortion linearization, else if transistors included in parallel, it comprises feedforward linearization. In later case power consumption reduced, because fundamental signals on transistors outputs are in-phase. Main drawback of this approach is high noise figure of weak inversion transistor.

In this paper we proposed design of bipolar amplifier based on feedforward/predistortion amplifier, comprising hybrid architecture, consisting from architectural elements on Fig.2(A) and Fig. 2(B). The main advantage of new amplifier is higher tolerance to chip manufacture process variation.

1-4244-0749-4/07/$20.00 @2007 IEEE.

II. Circuit-level Implementation

On the circuit level each gain element is represented by MOS or bipolar transistor. Fig. 4 and Fig. 5 show simplified circuits for high-frequency linearized amplifiers. Gain-nonlinearity tradeoff is done either by emitter or source degeneration inductors.

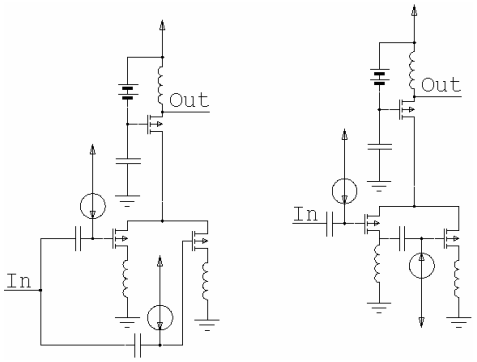

Figure 4. Schematics of advanced MOSFET linearized amplifiers. Left – feedforward linearized amplifier with high noise figure, right – predistortion/feedforward linearized low-noise amplifier.

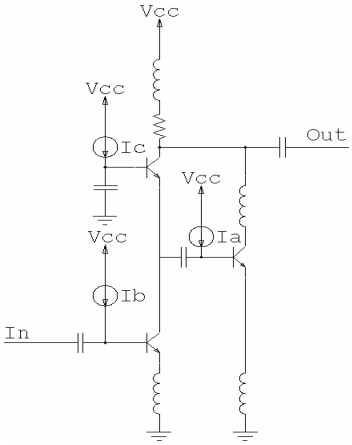

Figure 5. Proposed amplifier, based on predistortion/feedforward linearization architecture.

In proposed architecture design robust to variations of MOS transistor threshold voltage. Changes of bipolar transistors cutoff frequency are compensated due of automatic bias control. Bipolar amplifiers currents are subtracted on output, so gain is low (8dB) and power consumption high (80mW). But IMD3 suppression is about 40dB, overcoming the disadvantages. Fig. 5 shows the proposed highly-linear amplifier employing hybrid architecture of predistortion and feedforward techniques, where bias currents I_a and I_b are automatically stabilized by the means of buffer amplifiers. Buffer amplifier I_a have external tuning tap, intended for tuning between 5.2GHz and 5.8GHz operating bands.

III. Power and Linearization Efficiency of Feedforward/Predistortion Linearized Amplifier

Using most general block diagram from Fig. 1(A) and Fig.1(C), showing amplifiers dominated by 3rd-order distortion and assuming power consumption of each amplifier is directly proportional to transconductance of all its gain elements. We should take into account, what input signal power is neglected, i.e. $G >> 1$, so this power efficacy is not PAE, which is calculated in much more complicated way. The architecture on Fig.2(A) offer better power efficacy corresponding to + sign in equations (1) and (2). To separate scale effects from architectural improvement useful also to introduce parameter "output power per transconductor area with fixed power consumption". To obtain this rating for architectures on Fig. 1(A), 1(C) and 2(A) power consumption should be divided by active device area S, in general form

$$\begin{cases} \dfrac{P_{out}}{P_{cc}\,S} = \dfrac{\left(1 \pm \dfrac{1}{k^2}\right)}{1+k} \cdot \dfrac{1}{1+k} & k > 1 \\ \dfrac{P_{out}}{P_{cc}\,S} = \dfrac{\left(1 \pm \dfrac{1}{k^2}\right)}{1+k^{-3}} \cdot \dfrac{1}{1+k^{-3}} & k < 1 \end{cases} \quad (1)$$

$$\begin{cases} \dfrac{P_{out}}{P_{cc}\,S} = \dfrac{\left(1 \pm \dfrac{1}{k}\right)}{1+k} \cdot \dfrac{1}{1+k} & k > 1 \\ \dfrac{P_{out}}{P_{cc}\,S} = \dfrac{\left(1 \pm \dfrac{1}{k}\right)}{1+k^{-2}} \cdot \dfrac{1}{1+k^{-2}} & k < 1 \end{cases} \quad (2)$$

Equation (1) shows normalized power efficacy for feedforward amplifier, dominated by 3rd-order distortion, and equation (2) – for amplifier, dominated by 2-nd order nonlinearity. This case is particularly important, because developed amplifier nonlinearity is dominated by 2nd-order distortion. Raising (1) and (2) in power -1 we can obtain expression for normalized power consumption of feedforward amplifier, dominated by 2nd-order nonlinearity.

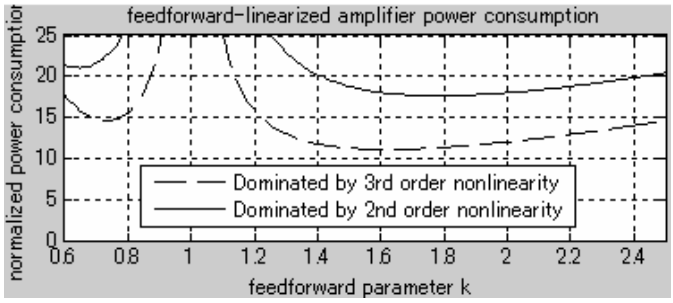

Figure 6. Normalized unit area power consumption of linearized feedforward amplifier. Graph built according to equations (1) and (2). Abscissa is the voltage gain of attenuator (k<1) (transconductance ratio between auxiliary and main amplifiers).

For 2nd-order distortion dominated amplifiers power efficacy reduce even more, and optimal value of feedforward parameter k shifted to 1.8 from k=1.63 optimal for 3rd-order nonlinearity dominated amplifiers. Simulated high-linearity amplifier had k=1.84, which is very close to optimal value in Fig. 6.

Simplified amplitude-balance equation for predistor-

tion/feedforward linearized amplifier, taking into account only quadratic and linear components, providing rude estimate of required distortion ratio between amplifiers 2 (named "G" and 3 (named "kG") in feedforward pair

$$Out2 = x(a_{1,1}a_{1,2} + 2a_{1,1}a_{0,1}a_{2,2} - a_{1,1}a_{1,3} + 2a_{1,1}a_{0,1}a_{2,3}) + x^2(a_{2,1}a_{1,2} + a_{1,1}^2 a_{2,2}) + k^{-1}x^2(a_{2,1}a_{1,3} + a_{1,1}^2 a_{3,1}) \quad (3)$$

First subscript index in Eq. (3) corresponds to order of nonlinearity (0- dc offset, 1 – linear gain, 2 – quadratic component and so on) and 2nd subscript index – identifier of gain element (1 - "Ga", 2 - "G", 3 – "kG" in Fig. 3). Writing out only quadratic component of output voltage, we can obtain equation (4).

$$a_{2,1}(a_{1,2} - ka_{1,3}) = -a_{1,1}^2(a_{2,2} - ka_{2,3}) \quad (4)$$

In conventional feedforward design [5], term $a_{2,2} - ka_{2,3} = 0$, representing ideal matching between amplifiers "G" and "kG" (referring to Fig. 1). In proposed design predistortion-related multipliers $a_{2,1}$ and $-a_{1,1}^2$ breaks degeneracy, so term $a_{2,2} - ka_{2,3}$ is no longer need to be exactly zero, although small value is still preferable. So exact matching of devices is of no concern for proposed architecture as long as one of the parameters of the predistortion amplifier (either nonlinearity or gain) is variable. Furthermore, because left and right sides of Eq. (4) have different multipliers before brackets, we can choose gain and nonlinearity of feedforward pair nearly arbitrary and still have a point of ideal nonlinearity cancellation, provided by bias tuning of predistortion amplifier 1 (named "Ga" in Fig. 3).

Tuning along with the compensation of carriers mobility variations helps to achieve stable 42dB of intermodulation suppression without strict requirements to transistors matching. Mismatch tolerance is greatest achievement of the proposed design compared with all previously published amplifiers, which were always mismatch-limited. Phase mismatch, determined by neglected delayed terms in Volterra series, was empirically tuned out and found to be small (3^0 of phase shift at all tuning range).

IV. Amplifier Design and Simulation Results

The amplifier shown on Fig. 3 was designed by the means of Agilent ADS and implemented on layout using Virtuoso Layout Editor by Cadence. Assura RCX program was used to extract the parasitic components of chip.Bonding wires SPICE parameters was extracted from previous measurements of packed chips and included into simulations. To control chip manufacture variation was added buffer amplifiers to bias transistors with external inputs. They change bias currents according to changes of charge carriers mobility, making design robust. With external bias tuning additional 20dB suppression of IMD3 products is possible [7]

On Fig. 7 we can see, what at 1.02 V of input voltage bias current become independent of carriers mobility of the chip. To stabilize main amplifier gain buffer amplifier input must be slightly below intersection point. In this case low carriers mobility cause decrease in bias current and thus increase in the main amplifier gain, compensating gain decrease caused by decreased carriers mobility. Best value for buffer amplifier input is estimated to be 0.99V, set by input resistive divider. This setting can be overridden by external voltage source.

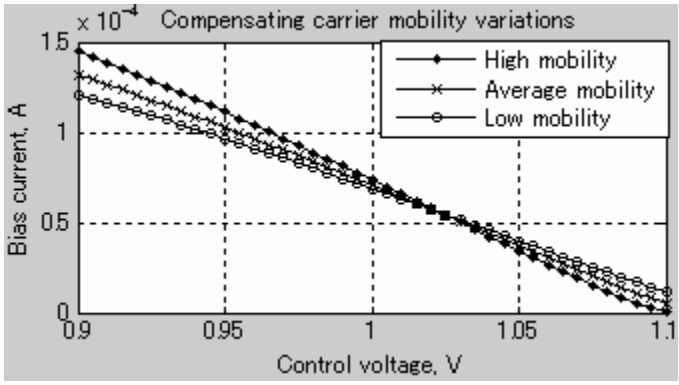

Figure 7. Bias current of main amplifier (uA) as function of bias voltage at the input of buffer amplifier. Two curves correspond to maximal (FF) and minimal (SS) possible carriers mobility in chip.

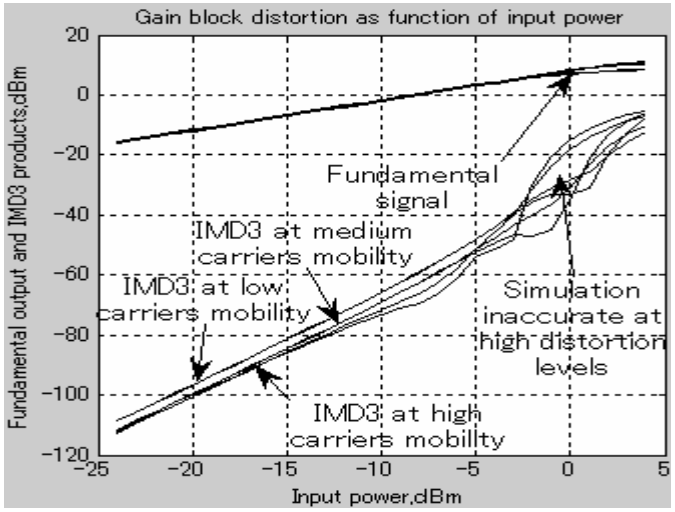

Figure 8. Two-tone simulation test of high-linearity amplifier at frequency 5.25 GHz. Shown fundamental signal (above) and IMD3 products(below).

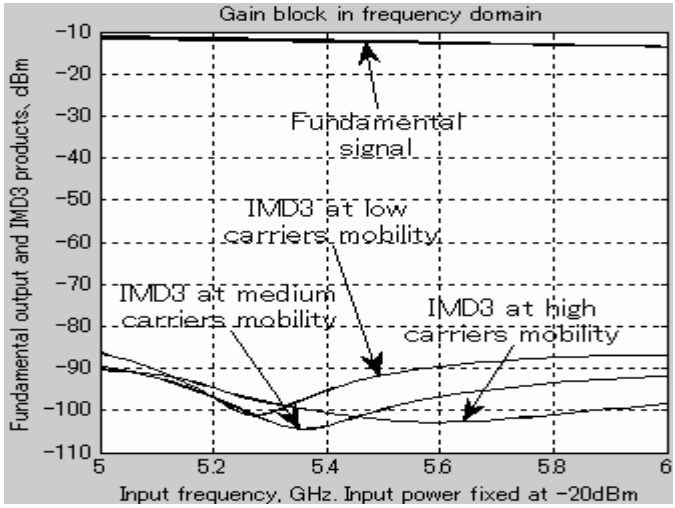

Figure 9. Two-tone simulation test of high-linearity amplifier in frequency domain. Shown fundamental signal (up) and IMD3 products (down).

2-tone 3rd order output products at frequency 5.25GHz as function of input power was simulated. Results consistent with OIP3 from +30dBm to +33dBm depending of chip manufacturing variation.

According to Fig.8 linearization works well at any input signal power up to 1dB gain compression point. This is advantage of the developed amplifier over typical predistortion designs. But the frequency bandwidth according to Fig. 9 remains a problem, 3dB linearization bandwidth may be as narrow as 200 MHz if centered at 5.25 GHz band. So implementation for dual-band systems (including 5.8 GHz systems) must include complicated tuning circuit.

During tuning test input power and frequency was fixed on 5.25GHz and -20dBm respectively. Tuning is expected to allow high-linearity operation in both 5.2GHz and 5.8 GHz frequency bands. Tuning affects mostly gain ratio in the feedforward pair of amplifiers, so frequency shift, defined by phase difference in feedforward amplifiers pair, is limited.

The area of amplifier prototype layout is 1 mm^2. Expected number of pins for stand-alone high-linearity amplifier is 24.

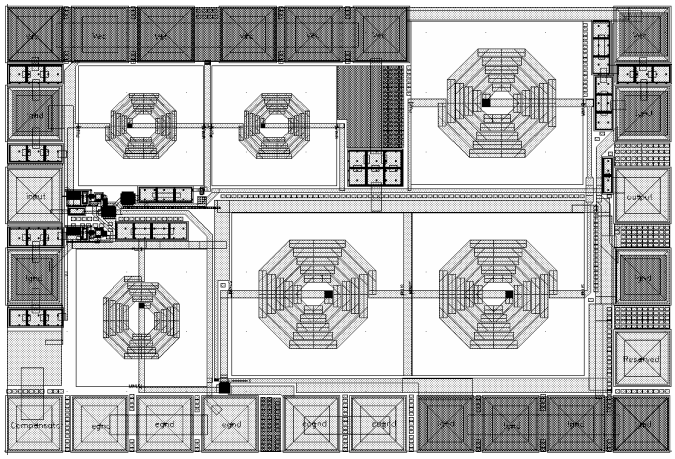

Figure 10. Layout of the high-linearity amplifier.

V. Conclusion

The high-linearity gain block was developed and simulated, including simulation of parasitic elements of chip layout. Verification of the proposed design and underlying theory experimentally is one of the most important topics of papers to follow.

Simulation results shown below in table 2. IIP3 for developed high-linearity amplifier is not specified, because this value strongly depends on power consumption – gain tradeoff thus not characterizing architectural improvement. For developed amplifier architecture typical IIP3=+25dBm.

Previously similar results for 5GHz frequency band was achieved only with expensive AlGaAs technology and with incomparable large power consumption [8]. Used in [8] approach was based on intrinsically highly-linear heterojunction transistors and simple predistortion linearization.

TABLE 2. PARAMETERS OF HIGH-LINEARITY AMPLIFIER

Parameter	No tuning, value	With tuning, value	Ref. [6]	Ref. [9]
OIP3, dBm	+30dBm - +33dBm	>+34 dBm	+32 dBm	+ 33.5 dBm
Gain, dB	>7.8dB	>7.5dB	11dB*	15.5dB
Power consumption	80 mW	87 mW	23 mW	45 mW
Noise figure	<5dB	<5dB	2.95dB	2.8dB
Operating frequency	5.15GHz – 5.825GHz	5.15GHz – 5.825GHz	0.9 GHz	0.9 GHz
1dB compression	+4dBm	+4dBm	-2 dBm	-5 dBm
IMD3 suppression	34dB – 40dB	>42dB	29 dB	26 dB

*without matching losses and at output impedance 100 Ohm

Developed amplifier have performance similar to 0.9GHz high-linearity amplifiers using 0.35um CMOS technology [9], but 5GHz operating band for 0.35um technology achieved in this design have no precedents. In this design reduced sensitivity of amplifier to variations of MOSFET threshold voltage. Variations of charge carriers mobility are also compensated in current design, resulting in higher possible production yield.

ACKNOWLEDGEMETS

This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration with Agilent Technologies and Cadence Corporation.

REFERENCES

[1] Minh T. Le and L. Thibault, "Performance Evaluation of COFDM for Digital Audio Broadcasting Part II: Effects of HPA Nonlinearities," *IEEE Transactions on Broadcasting, vol.44, No.2, pp. 165-171, June 1998.*

[2] M. Kuipers and R. Prasad, "Pre-Distorted Amplifiers for OFDM In Wireless Indoor Multimedia Communications," *IEEE Annular Vehicular Technology Conference, pp. 395-399, 2000.*

[3] C. W. Fan and K. K. M. Cheng, "Amplifier Linearization using Simultaneous Harmonic and Baseband Injection," *IEEE Microwave and Wireless Ccomponents Letters, vol. 11, No. 10, October 2001.*

[4] J. Kang, J. Yoon, K. Min et al., "A Highly Linear and Efficient CMOS Power Amplifier With Harmonic Control," *IEEE Journal of Solid-state Circuits, No. 6, , pp. 1314-1322, June 2006.*

[5] Y. Ding and R. Harjani, "High-Linearity CMOS RF Front-End Circuits," *Springer*, Library of Congress, USA, 2005.

[6] S. Ganesan, E. Sanchez-Sinencio and J. Silva-Martinez, "A Highly Linear Low-Noise Amplifier," *IEEE Transactions on Microwave Theory and Techniques, vol.54, No.12, pp. 4079-4085, December 2006.*

[7] T. Y. Yum, L. Chiu, C. H. Chan and Q. Xue, "High-Efficiency Linear RF Amplifier – A Circuit Approach to Achieving Compactness and Low Distortion," *IEEE Transactions on Microwave Theory and Techniques, vol.54, No. 8, pp. 3255-3266, August 2006.*

[8] C. H. Lin, H. Z. Liu, C. K. Chu et al., "A Single Supply, High Linearity 2-W PA MMIC for WLAN Applications Using Quasi-Enchancement Mode PHEMTs," *IEEE Microwave and Wireless Components Letters, vol.. 16, No. 11, pp. 618-620, November 2006.*

[9] Y. Ding and R. Harjani, "A +18dBm IIP3 LNA in 0.35um CMOS," *IEEE International Solid-State Circuits Conference, pp. 165-167, 2001.*