High Dynamic Range Mixer in CMOS 0.18 um Technology for WLAN Direct Conversion Receiver

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***Abstract*-This paper describes simulation results of high dynamic range mixer, based on resistive ring topology. Mixer is designed using TSMC CMOS 0.18um technology. This mixer downconverts RF signals in the range 2-6 GHz to low IF using LO signals below corresponding RF frequencies and perform low-pass filtering with 3dB bandwidth 33 MHz. Unlike pure resistive ring topology, mixer has a positive power gain. Output 2nd and 3rd order intercept point for proposed mixer is 41dBm and 22dBm, resulting in dynamic range over 60dB even for high-throughput transceivers. Mixer have an integrated LO drive with gain 6dB, so does not require significant LO power to operate. The mixer has DC power consumption 54mW and can be used in the most demanding ultra-wideband OFDM radio and WLAN communication systems.**

I. INTRODUCTION

In the modern wireless communication networks two standards are becoming increasingly popular. First is 802.15.3 High Rate WPAN, and second is 802.11 WLAN.

Both standards are using OFDM scheme to increase data throughput. But one of the main problems of OFDM system remained inter-channel interference. For WLAN desirable adjacent channel rejection is about 60dB, and for WPAN due to larger number of OFDM channels requirements are even more strict. ACPR requirement necessitate high-linearity solution for entire transceiver, including mixer. Linearity of common workhorse of RF transceivers, Gilbert cell mixer is not satisfactory in modern communication systems. Although in [1],[2],[3] was proposed some solutions to increase linearity of wideband Gilbert cell mixer, all of these solutions still have dynamic range around 30-40dB and thus unsuitable for WPAN communication or even for broadband WLAN communications. Now industry chiefly needs wideband, high-linearity mixer. Wide known resistive ring mixer meets both requirements, but have significant drawbacks - conversion loss and high LO power。

In the proposed design both problems are alleviated, but DC power consumption is slightly increased. Also using analog postdistortion technique, linearity of mixer is further boosted by approximately 10dB, and first time low-pass filter implementation is based on skin-effect induced loss. This is the first time a filter with cutoff frequency as low 33 MHz implemented on-chip without using noisy active elements, resulting in superior noise figure 11.5dB at IF 10MHz. Superior noise performance makes proposed mixer suitable for direct conversion receivers.

II. COMPOSITION OF MIXER

The mixer comprises of the following key components: RF matching circuit, LO differential power driver, resistive ring mixer core, postdistortion amplifier, low-pass filter as shown in Fig. 1.

Postdistortion amplifier is implemented using matched pair of cascode amplifiers. Low-pass filter consists of 2 identical LC pi-sections. Cutoff of the low-pass filter is determined by skin effect equation so ultra-thick top metal of filter inductors (see Fig. 2) is necessary to reduce cutoff frequency of the filter.

Postdistortion amplifier make use of different sign of quadratic nonlinearity at weak inversion and strong inversion for deep-submicron MOSFET transistors. Transistors of resistive ring is biased into strong inversion region, while transistors of postdistortion amplifier biased into weak inversion region, thus nullification of quadratic distortion is possible.

Figure 1. Block diagram of proposed high dynamic range mixer

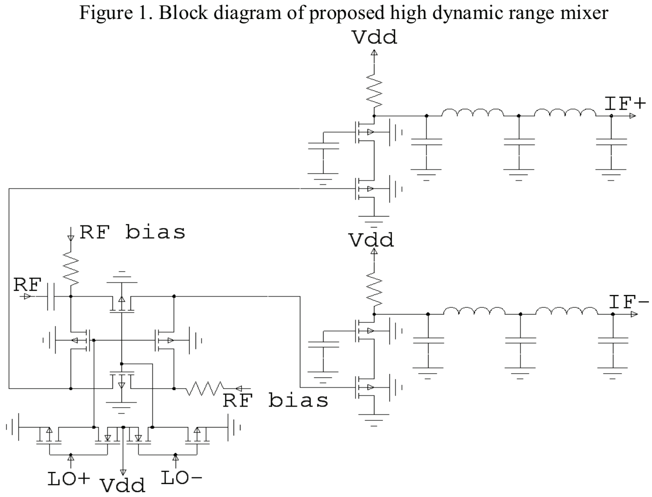

Figure 2. Simplified schematic of proposed high dynamic range mixer

III. Simulation results

Because output of mixer is usually high-impedance, effort should be made for large and flat voltage gain. But proposed mixer was optimized not for gain flatness, but for minimal noise figure. Because mixer is most noisy at high frequency, gain optimized to be maximal close to maximal operating frequency (see Fig. 3). For same reason the size of resistive ring transistors was increased compared with [4] 4-fold. Resulting degradation of bandwidth allowed dramatic reduction of in-band noise figure. (see Fig.4)

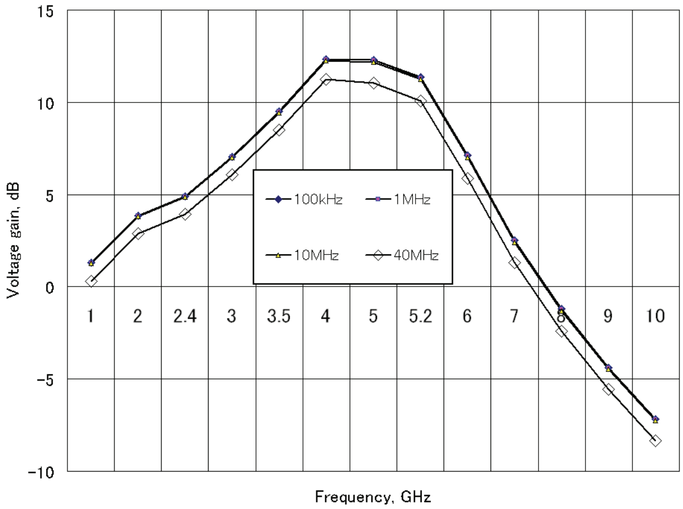

Figure 3. Voltage gain of high dynamic range mixer, dB (simulated post-layout)

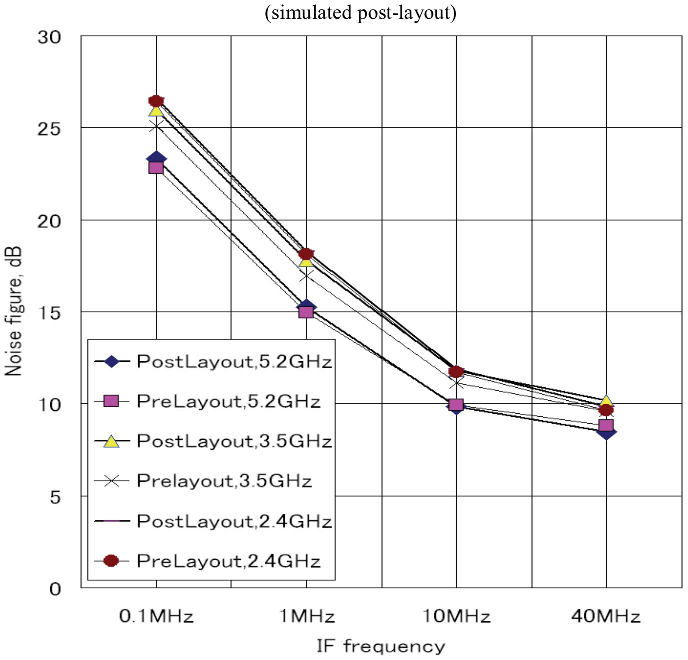

Figure 4. Noise figure of high dynamic range mixer, dB (simulated)

Thermal noise floor of mixer is 8dB and flicker noise corner frequency estimated to be 6MHz. The 70% of flicker noise attributed to postdistortion amplifiers and 25% to resistive ring mixer core. Other 5% comes from local oscillator driver.

Thermal noise is dominated by the resistive ring core, leaving only a small contribution to RF matching circuit and LO driver. Along with preceding LNA, having 2.5dB noise figure and 15dB gain, RF front-end noise figure can be kept below 4dB at IF 10MHz and above, making mixer very attractive for direct conversion architecture. If the minimal IF frequency is set to 1MHz, overall RF front-end noise figure still can be below 5.5dB.

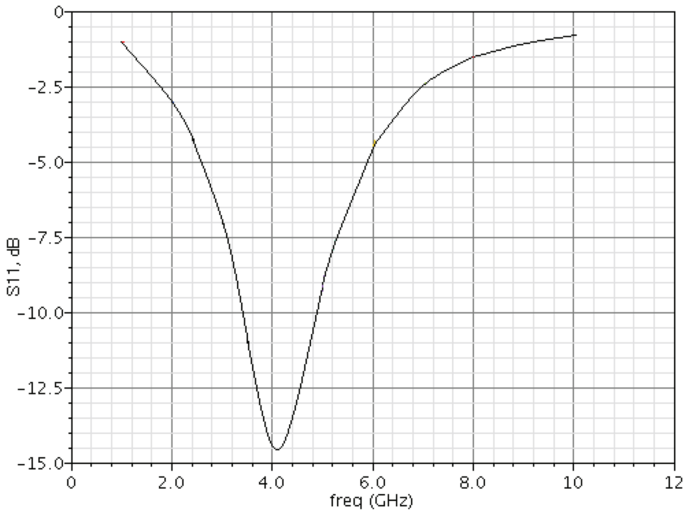

Figure 5. Input return loss of high dynamic range mixer, dB (simulated post-layout)

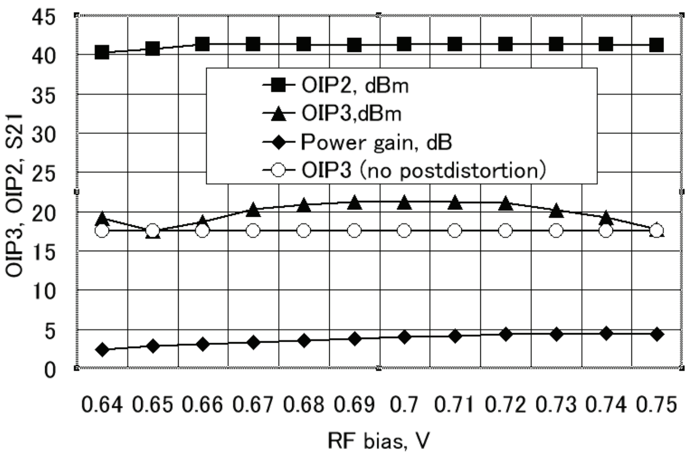

Figure 6.Power gain and intercept points of high dynamic range mixer (simulated post-layout)

The input matching (see Fig. 5) for proposed mixer is narrowband. Wideband matching was considered impractical, because unlike LNA connected to strongly reflecting antenna, mixer is connected to weakly reflecting output of LNA. So large input reflection do not hamper stability and can be tolerated as long as noise matching is close to optimal. Simultaneous gain and noise matching is not implemented mixer design not to increase passive components count.

On the plot of worst-case intercept points (see Fig. 6) clearly visible peak of the OIP3 at RF bias around 0.7V. Amplitude of peak is 5dB, corresponding to 10dB linearization of resistive ring mixer. This confirmed by large figure-of-merit characterizing linearity.

$$FOM = \frac{OIP3}{P_{DC} + P_{AC}} = \frac{158mW}{67mW} = 2.4$$

Linearization of mixer is caused approximately 1dB gain loss and 1dB noise figure increase, but it is compensated by 10dB increase of dynamic range. Taking into account thermal noise and distortion of following sample-and-hold circuit, optimal input power for proposed mixer is -20dBm. At this input power dynamic range is limited by 2nd order distortion, with 3rd order distortion making significant contribution only if input RF power more then -6dBm.

In [4], was proposed to use output buffer, but authors did not used output buffer as means of linearization. Instead buffer was used only to compensate large conversion loss of small transistors in ultra-wideband resistive ring.

In [5] design of mixer had good linearity, but limited by the large leakage of LO signal. So combining low-pass filter and postdistortion amplifier addressed both major issues in designs [4] and [5].

In [6] was proposed to use alternative approach to linearization, i.e. bootstrapped switch. Although performance of bootstrapped linearizer is close to postdistortion linearizer, the disadvantage was the huge bandwidth reduction, typical for bootstrapped switches.

Table 1. Comparison of wideband mixers

Parameter	Work [4]	Work [5]	Work[6]	This work
Voltage gain	-7.5dB	-5.8dB	>8dB	>+3dB
Bandwidth	1-11GHz	0.9-1.8GHz	2.3-2.6GHz	2-6GHz
Noise figure @IF	7.5dB @10MHz	5.8dB	11dB @7MHz	11.5db @10MHz
LPF cutoff	-	-	-	50 MHz
DC power	3mW	0	0	54mW
LO power	8mW	25mW	≈ 25mW	13mW
OIP3	+4dBm	+13.8dBm	0dBm	+22dBm
OIP2	not known	not known	not known	+42dBm
Linearity FOM	0.2	1	0.04	2.4
Dynamic range	48dB(IM3)	43dB(LO leakage)	40dB (IM3)	>58dB (IM2)

Table 1 illustrates proof what proposed mixer composition is superior in signal fidelity over all competing mixers. Signal dynamic range was calculated assuming RF input power -20dBm.

Table 2. Technical parameters of proposed high dynamic range mixer

Parameter	Value
Input return loss	<-10dB
Chip area (2 sizes of LPF possible)	2 mm^2 or 3 mm^2
1dB IF output compression point	+1 dBm
Supply voltages	1.8V power and 0.7V bias
IF output maximal voltage swing	0.8V p-p

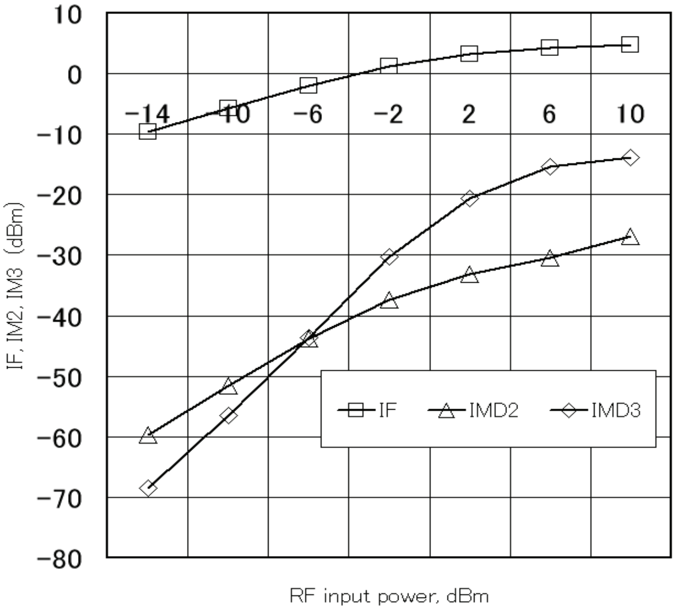

Figure 7. IF signal and main contaminating signals at the output of high dynamic range mixer

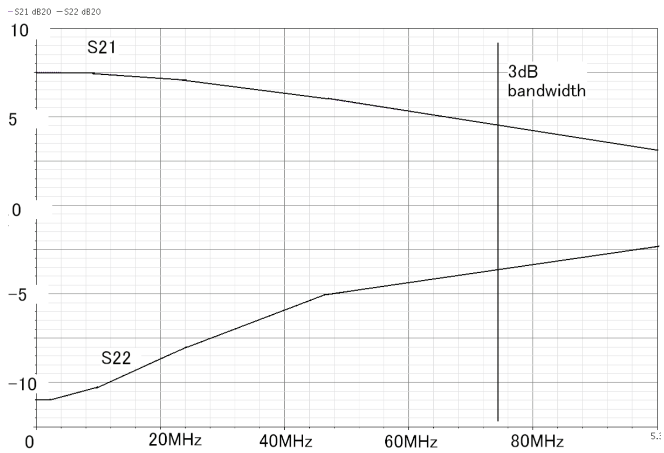

Figure 8. IF power gain and output return loss as function of IF frequency for 66MHz LPF.

Mixer was designed and sent to fabrication in 4 variants – with 33MHz or 66MHz low-pass filters, and also with compact LO drive, requiring 13mW input power or high-gain LO drive with digital phase splitter. Low-pass filter cutoff is shown on Fig.8.

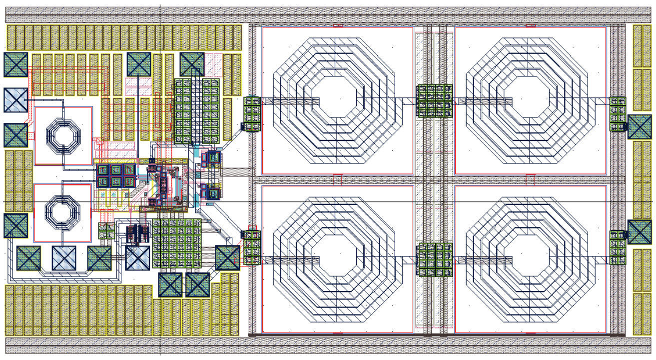

Figure 9. Layout of wideband mixer with integrated LO phase splitter and 66MHz low-pass filters. Total chip area 3mm2

Although high-gain LO driver improve integration of mixer solution, with 0.18um Si CMOS technology it expected to limit maximal operating frequency to 4GHz, because classical digital drivers fail to propagate signal at frequencies above 4GHz, if 0.18um TSMC CMOS technology is used. So LO driver become the bandwidth-limiting factor for proposed mixer.

1dB output compression point for mixer lies at +1dBm (see Fig. 7), what confirms reliability of -20dBm optimal input power point for the mixer. But the mixer can also work at RF input power as high as -6dBm and still have 40dB dynamic range.

IV. CONCLUSION

A 0.18um CMOS mixer, based on resistive ring topology was designed, simulated and sent for fabrication. The mixer has a large bandwidth covering from 2GHz to 6GHz and suitable for direct conversion receivers. The chip area, including 66MHz low-pass filter, is $3mm^2$ (see Fig. 9) Proposed mixer have an OIP3 more then +22dBm and OIP2 more then +41dBm. Unlike more conventional mixers, dynamic range limited by IM2 instead IM3. For IEEE 802.15.3 systems (WPAN) distortion is equal to thermal in-band noise leaving no reasons to reduce IM2 and IM3 further. Proposed mixer is suitable for WLAN and WPAN wideband communication systems with strict requirements for dynamic range. Dynamic range of mixer reaches 60dB.

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