Design of Flat Gain and Low Noise Figure LNA for 3.1-10.2GHz Band UWB Applications in 0.18um CMOS Process

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Abstract

This paper shows the design of a broadband low noise amplifier (LNA) for ultra-wideband (UWB) system on 0.18um CMOS process. The proposed LNA uses resistive shunt feedback technique and an inter-stage inductor as an inductive peaking to realize the flat gain throughout the UWB band. The designed UWB LNA has a noise figure lower than 3.5dB, gain above 20dB in the frequency range 3. 1-10.2GHz. It consumes 24mW from a supply voltage of 1.8V.

Keywords: LNA, UWB systems, 0.18um CMOS Process, Flat gain.

1. Introduction

Ultra-wideband (UWB) system [1] is a new wireless technology capable of transmitting data over a wide spectrum of frequency bands from 3.1-10.6GHz with very low power and high data rates and even at very low cost [2]. The possible applications of UWB technology can be applied in imaging systems, sensor networks, wireless personnel area network (WPAN) and so on. In particular, it is envisioned to replace almost all cable networks at home or in an office with a wireless connection that features hundreds of megabits of data per second.

The design of a UWB low noise amplifier (LNA), which is a critical block in the receiver, faces several challenges such as wide-band input matching, linearity, sufficient gain, low noise figure (NF) and low power consumption because it should achieve high gain to suppress the noise from the subsequent stages. Among the UWB LNA's architecture proposed so far in CMOS technology, distributed amplifiers can realize the gain-band width product (GBW) very close to device f_t, but it occupies very large chip area and consumes very high power [3]. A multi-stage LC ladder network can realize wideband input matching, but power consumption worsens, and insertion loss of filter network adds noise at high frequency [4]. Resistive shunt feedback is a widely known technique in wideband amplifiers [5], but it is hard to satisfy the flat gain and noise performance simultaneously throughout the UWB band [6].

In this paper, a resistive feedback and an inductive peaking technique is employed to achieve the flatness of the gain throughout the UWB band. Negative feedback also improves the stability (K-) factor to provide unconditional stability of the amplifier and reduce the gain sensitivity. An inter-stage inductor which acts as an inductive peaking, to further stabilizes the flatness of the gain beyond 5GHz.

2. Circuit Design

In source degeneration topology which is widely used structure for narrowband LNA design [7], the frequency responses of NF are controlled by quality (Q-) factor of the inductors at input-matching circuit and source-degeneration branch, and it is necessary to choose Q as close to the maximally flat condition as possible which is usually not possible on Si-substrate. Furthermore, quality factor of two inductors (input matching and source degeneration branch) influence the resonance frequency of input matching, therefore it is difficult to achieve wideband matching due to the source degeneration topology alone. Therefore, a feedback technique is employed to achieve wideband matching in this paper and the source-degeneration inductor is realized by bonding wires to obtain a flat Q_{in} in order to achieve the excellent NF flatness of the designed LNA throughout the UWB band and the results will be discussed later.

The designed LNA circuit can be divided into three parts; cascode amplifier with shunt resistive feedback stage, inter-stage network, and cascaded with inductive peaking amplifier stage. The schematics of UWB LNA is shown in Fig. 1, and the supply voltage is 1.8 V. The DC blocking capacitors are C1 and C2. For input stage, a cascode amplifier with resistive shunt feedback is used which have high reverse isolation and frequency response. The feedback resistance supplies feedback current to the input so that a suitable value of shunt feedback resistor (R1) can be selected to achieve input matching, a low NF, and also broadband gain, simultaneously.

The third stage is common source with shunt inductive peaking L3 to achieve high gain at higher frequency, also have resistive shunt feedback (R2) to extend the bandwidth and flattens the gain. Inductor L4 is used to achieve output matching.

Figs. 2 and 3 show the method of optimization of the value of R1 to achieve flat high gain and low NF. In the figures, gain and NF are improved as the value of R1 increases because of the feedback current. From the graph, the best value of R1 was selected to give maximally flat gain and low NF. Similarly, Figs. 4 and 5 show the effects of R2 on the gain and NF. It is noted in Fig. 5 that the in-

fluence in NF due to the change in values of R2 is minimum but in Fig. 4, the effects in gain are more noticeable.

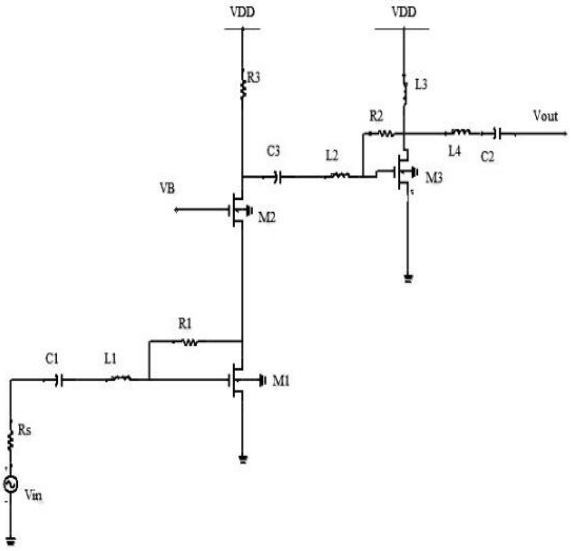

Fig. 1. Designed UWB LNA with resistive shunt feedback technique and inductive peaking technique.

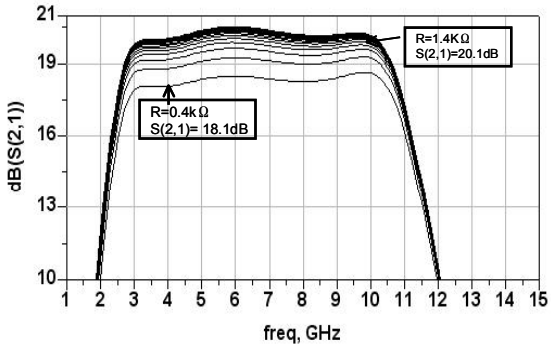

Fig. 2. Effects of R1 on gain.

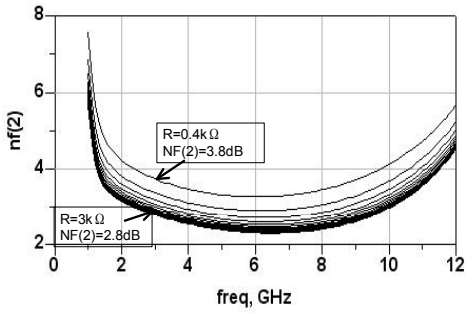

Fig. 3. Effect of R1 on NF.

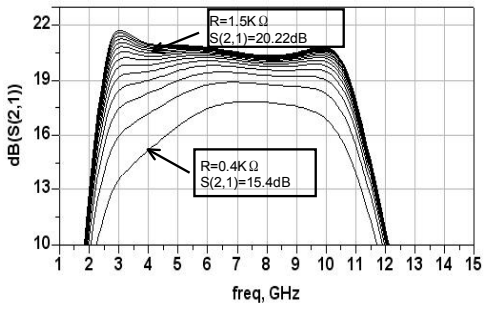

Fig. 4. Effects of R2 on gain.

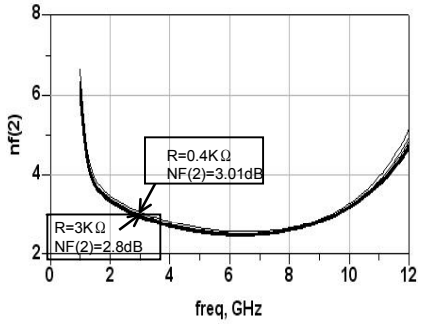

Fig. 5. Effects R2 on NF.

3. Simulation Results

Fig. 6 shows the effect of inter-stage inductor (L2) on gain where gain in high frequency degraded to approximately the half of maximum gain without L2. The inter stage network consists of serial capacitor and inductor which make series resonance at the middle of the frequency range, that contribute of further extension of the band width (BW) of this LNA.

Thus, the optimized values of the final design of the proposed architecture has bandwidth from 3.1-10.2 GHz based on 0.18μm CMOS 1P6M technology. The gain flatness is 20 dB and noise figure is less than 3.5dB throughout the band which is also plotted in Fig. 6. The simulation result of input matching (S_{11}) is shown in Fig. 7 where S_{11} is lesser than -7 dB in the frequency ranges of interest. Fig. 8 show the reverse isolation of the designed LNA which is lesser than -45dB. The third order intercept point are estimated at 8GHz and shown in Figs. 9.

One of advantages of the designed LNA is flatness of the gain, and low NF. This LNA has better performance than LC-Ladder type input matching network [4] or distributed LNA [3], so Table 1 shows comparison of the per-

formance of this work with others on 0.18um CMOS Process only. The previous topologies have high NF at high frequency but this topology has very flat gain and noise figure over the full band from 3.1 to 10.2 GHz. The layout of the proposed UWB LNA is presented in Fig. 11. The die area including the pads is 0.97mm x 0.7mm and this layout is already taped out for fabrication.

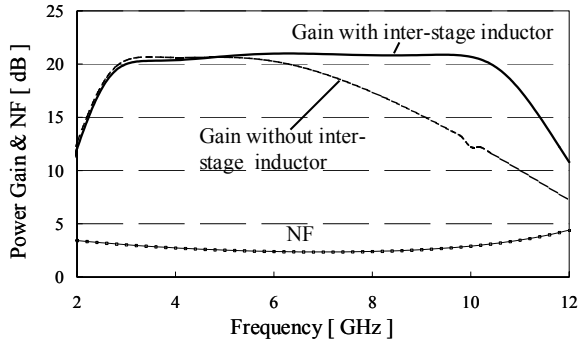

Fig. 6. Effects of inter-stage inductor on amplifier gain.

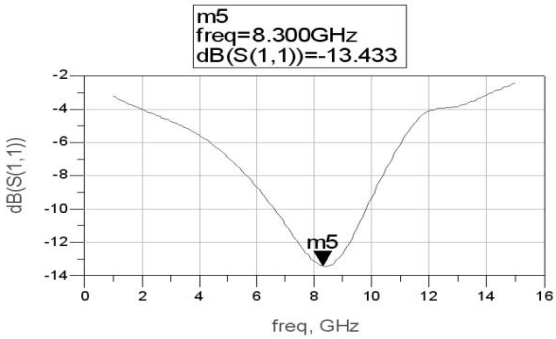

Fig. 7. The input return loss of designed UWB LNA.

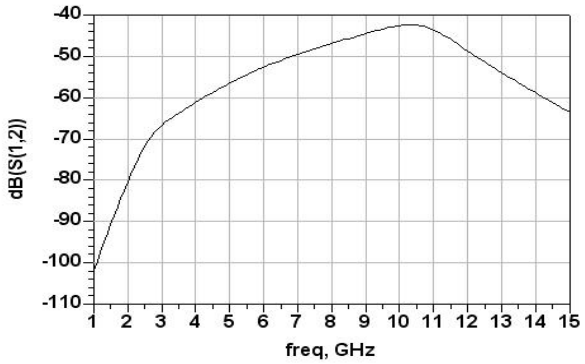

Fig. 8. Reverse isolation (S12) of the designed UWB LNA.

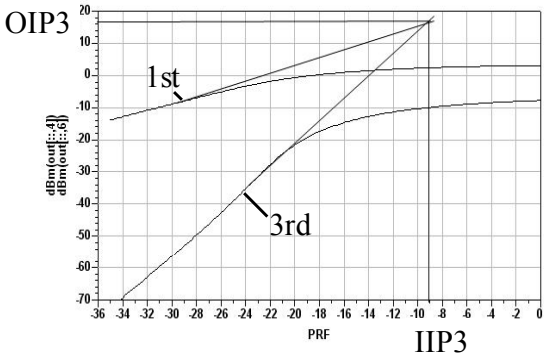

Fig. 9. The third order intercept point of the designed UWB LNA.

Table 1 Comparison of UWB LNA Performance: published and present work.

	Ref.[8]	Ref.[9]	Ref.[10]	**This work**
Gain(dB)	10	9.5	9.7~7.5	20
Noise figure(dB)	4	5-5.6	4.5~5.1	3.5
Bandwidth (GHz)	2.3~9.2	3.1~10.6	3.1~10.6	3.1~10.2
Power dissipation (mw)	9	9.47	29	24
Third order intercept (dB)	-6.7	-13	-6.2	-9
Technology	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS

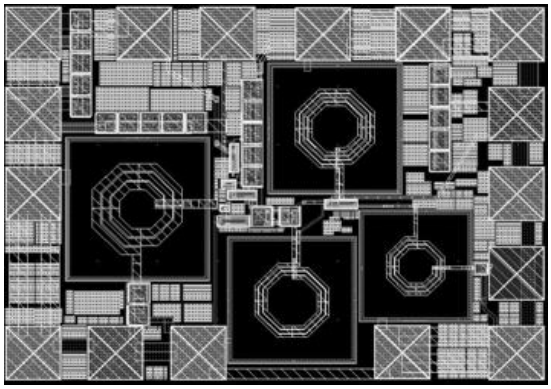

Fig. 10. Layout of the designed UWB LNA on 0.18um CMOS process. (Already taped out for fabrication).

4. Conclusion

A CMOS UWB LNA with a resistive shunt feedback and an inter-stage inductor to further stabilize gain flatness has been designed and fabricated using a 0.18um CMOS 1P6M process. The UWB LNA exhibits a 20 dB flat gain, NF less than 3.5dB, input return loss is less than -7 dB, -9dBm IIP3, and 24 mW power consumption over a 3.1–10.2 GHz range. Due to the flatness of the gain, phase linearity has significantly improved (though phase linearity has not been discussed in this paper). This in turn, finds a suitable for the DS (Direct Sequence code division multiplexing scheme)-UWB applications [6]. The designed chip has already been taped out for fabrication and the measured results to verify the design is important which is taken as one of the priorities works in near future.

Acknowledgment

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