Design of Highly Linear, 1GHz 8-bit Digitally Controlled Ring Oscillator with Wide Tuning Range in 0.18um CMOS Process

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Abstract: **This paper presents a simple architecture for 8-bit digital controlled oscillator (DCO) on 3-stages ring topology in TSMC 0.18um CMOS technology. A new schematic of tristate inverter is also proposed. The proposed tristate inverter has higher switching speed and low power consumption as compared to conventional one. The control digit changes the driving current that provides large tuning range from 316 MHz to 1165 MHz with very good linearity. The output voltage swing is always greater than 1.6V while the supply voltage is 1.8V. The proposed DCO has simulated phase noise of -114dBc/Hz @1MHz and 23.2mW power consumption at 1.0 GHz central frequency.**

Index Terms **— ring oscillator, DCO, inverter, phase noise, linearity, power consumption.**

I. INTRODUCTION

In recent years, CMOS technology is scaling down resulting to a very low control voltage that leads to the availability of only very steep slope [1], and this complicates the implementation of conventional RF circuits in CMOS technology, often causes instability and the portability issues. Furthermore, low voltage and thin metal interconnects which are achieved in a scaled-down CMOS process are advantageous to digital circuits but the same becomes disadvantages to RF circuits due to reduced voltage headroom, low inductor's quality factor, and reduced gate oxide reliability. Therefore, RF circuits such as RF oscillators need to be realized employing digitally controlled logics for future generation wireless technology.

In conventional wireless systems, two types of oscillators i.e. ring oscillator and LC-tank oscillator are often used to generate a local frequency in a phase-locked loop (PLL) [2]. The ring oscillator is often used in MHz frequency applications because of its compactness, as spiral inductors are usually not necessary in a ring topology. In GHz frequency applications, the later is usually preferred because of its improved noise performance and lower power consumption.

As a ring oscillator is more compact than LC-tank oscillator, designing a ring oscillator for GHz frequency applications is the main area of interest in this paper. In Ref. [3], the architecture uses transmission gate between inverter delay stages and vary the value of the resistance of the transmission gate with the control voltage applied to the transmission gate which has drawback of frequency saturation for higher voltages so that it provides low control voltage range. In Ref. [4], [5], digital control but asymmetrical stages were used which reduces the output voltage swing that makes the circuit sensitive to the phase noise. In Ref. [6], parallel resistors were used in transmission gate and control the resistance by changing digital control. It provides high load resistances means more power dissipation. And also resistance becomes saturated at high control logic so that linearity worsens.

This paper proposes a new architecture for 8-bit digitally-controlled ring oscillator. This architecture provides symmetrical load, high linearity and very large output voltage swing which overcomes the problem of Ref. [4], [5]. The output frequency of the DCO is controlled by the varying the driving current according to the input control bits.

II. DESIGN OF CONVENTIONAL RING OSCILLATOR

A basic ring oscillator uses odd number of inverters. An example of three-stages ring oscillator [2] is shown in Fig 1. Each inverter in the oscillator is used as a delay cell. The frequency of oscillation for identical cell is given by Equation (1).

$$f_{osc} = \frac{1}{2N\,T_d} \tag{1}$$

Where T_d is the delay of each inverter cell and N is number of identical cell. From Equation (1), the period or frequency of oscillation is varied either by changing the number of inverter stages in the ring or varying the propagation delay of inverter. The delay of each inverter cell is further expressed as,

$$T_d = \frac{C_L \cdot \Delta V}{I_d} \tag{2}$$

Where C_L is load capacitance, ΔV is the output voltage swing and I_d is the driving current to the load. It is clearly noted from the Equation (2) that the frequency of oscillation without changing number of stages can be varied either by changing the load capacitance or

driving current to the load. The propagation delay of inverter is proportional to Width to Length (W/L) ratio of the transistor as increment in width increases the capacitance and decreases the resistance that makes time constant equal and frequency remains constant. The load capacitance (C_L) at the output node of inverter can be expressed by Equation (3) [7].

$$C_L = C_{gsM3} + C_{gsM4} + C_{dbM1} + C_{dbM2} + C_{gdM1} + C_{gdM2} + C_w \quad (3)$$

Where, suffices g, s, b represent gate, source and body (substrate) of transistors M1, M2 and M3, respectively. Similarly, C_w represents wire capacitance. The load capacitance can be changed by using MIM capacitor or MOS transistor at the output node of inverter. But it cannot be much useful in sub-micron technology as wired capacitance have significant portion in load capacitance, which in turn, limits the maximum oscillating frequency [6] of an oscillator. Thus, this approach would not be much useful to achieve wide turning range of an oscillator. Controlling delay by changing the driving current (I_d) would support for wide tuning range and also provides high linearity which is utilized in the presented DCO.

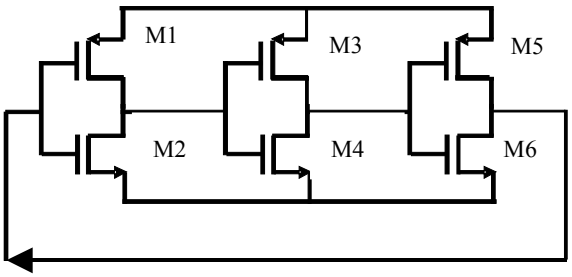

Fig. 1. Three-stages conventional ring oscillator [2].

III. DESIGN OF PROPOSED DCO

A. Topology of DCO

The figure showing the principal of the proposed 3-stages digital controlled ring oscillator is shown in Fig 2. The DCO consists of control signals, driving current (I_d), charging path, discharging path and load capacitance (C_L) as circuit elements where output frequency is varied varying the driving current (charging and discharging current) according to the control bits. The circuit has 8 control bits (D0-D7). All the stages are identical and make a ring for an individual bit. For 8 bits, 8 rings with different W/L ratio are made in parallel by connecting them at the output of each delay cell. Each ring is made with identical stages to provide equal delay. One of the advantages of the proposed method is that it provides symmetrical load unlikely in ref. [3-5]. The output frequency of the oscillator depends on the control bits. The proposed schematic has used newly proposed tristate inverter for the delay cell.

B. Tristate Inverter DCO Cell

Fig. 3 shows the schematics of the proposed DCO and tristate inverter circuit used. The proposed tristate inverter uses four transistors whose numbers are equal to the conventional one but differs in topology. In conventional inverters, four inverters gate are connected in series.

In the proposed inverter, it has control input D that controls the signal propagation from input to the output through transistors M7 and M8 or M9 and M10 depending on the input level Low (0), High (1), respectively. When D=0, the output will no longer connected to the input and none of the transistors M9, M10 conducts. The size of the transistors is selected to provide equal delay through both the paths. The W/L ratio of all the transistors is listed in Table 1.

Table 1: Size of the transistors in tristate inverter.

Name of Transistors	M1	M2	M3	M4
Size ratio	2.5	1.0	2.5	1.0

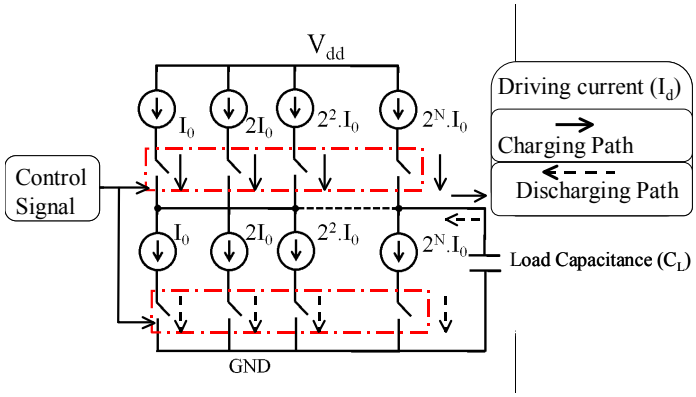

Fig. 2. Demonstration of the working principle of DCO.

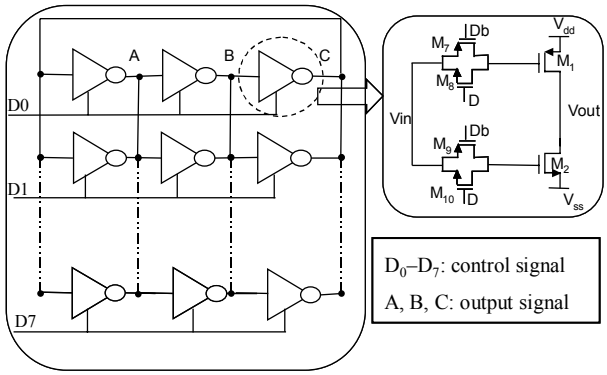

Fig .3. Schematics of proposed DCO and unit cell of inverter.

For one delay cell calculation the signal starts propagating at node V_{in} and terminates at node V_{out} through node B. Hence, from the equivalent circuit of Fig. 4, the delay of the tristate inverter cell can be interpreted

terpreted in to two parts: inverter delay and transmission gate delay. The total delay of the circuit is given by,

$$T_d = T_{INV} + T_{TG} \quad (4)$$

Hence, inverter cell delay (T_{INV}) is calculated by Equation (2) where the driving current (I_d) is given by Equation (5) for the proposed oscillator.

$$I_d = I_0 \bullet \sum_{n=0}^{n=N-1} \left(\frac{W}{L}\right)_n B_n \quad (5)$$

Where I_0 = Current flowing for W/L=1, B_n is the status of the control bits i.e. B_n =1 if switch is on, and B_n = 0 if switch is off. It was also explained before that output frequency is controlled by changing I_D in the proposed DCO as it provides high linearity for a very wide tuning range in comparison to the change in load capacitance as earlier employed in [4].

The transmission gate can be represented as a constant RC delay cell [7] where the delay for the transmission gates is given by,

$$T_{TG} = 0.69 R_{TG} C_{LB}$$

Where R_{TG} is the resistance of the transmission gate, approximately constant during switching but inversely proportional to the W/L ratio of the transistors and C_{LB} is the load capacitance at the output node of transmission gate.

The equivalent circuit representing delay control mechanism of the proposed DCO is shown in Fig. 4 where inverter transistors are shown by current sources, transmission gate as a constant delay cell (TG) and control input is represented by switches in current sources. The load capacitance (C_{LA}) of the inverter is constant because all the transistor are connected to that node irrespective of the number of control bits status. According to the control code (D0-D7), switches turns on or off and set the value of current which controls the delay and in turn, the oscillating frequency.

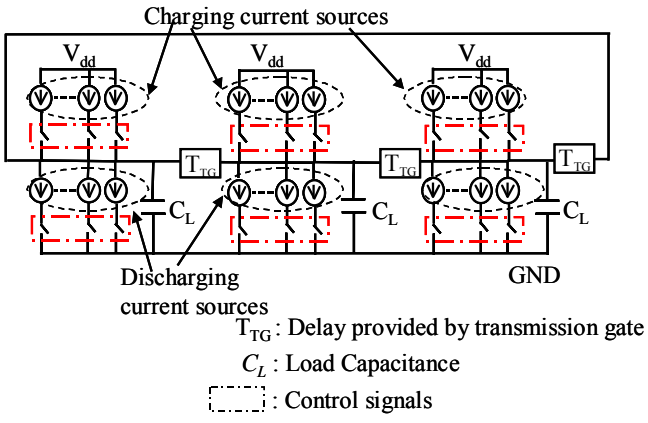

Fig. 4. Equivalent circuit of the proposed DCO.

IV. SIMULATION RESULTS

The proposed DCO was designed by means of ADS (Agilent Co., ADS 2006) using TSMC 0.18um CMOS process parameters, and supply voltage of this process is 1.8 V.

The comparison of voltage transfer characteristics of proposed and conventional tristate inverter circuit shows that shows that proposed tristate inverter has 20-30% power reduction from 2GHz to 250MHz frequency. It also shows the significant improvement of 20% in speed.

The proposed DCO was simulated for all the possible combination of control code. The frequency range of the DCO is from 316MHz to 1165MHz. The frequency versus input control words is shown in Fig. 5, where it is noted that the proposed DCO possess the high linearity for the wide range of frequency.

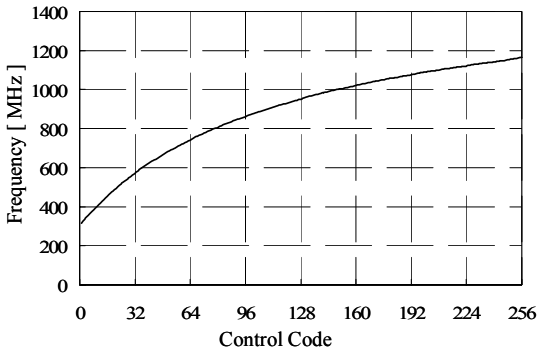

Fig. 5. Relationship between central frequency and input control code showing linearity of the designed DCO.

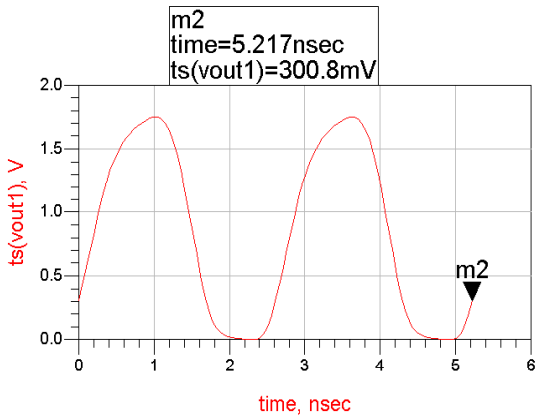

Fig. 6. Time-domain waveform of output voltages.

The simulated output waveform of the selected control input signal is shown in Fig 6. This clearly shows the large output voltage swing (>1.6V). The proposed DCO also changes the output frequency within one clock period without any ringing at the output voltage

also output voltage swing is constant. Phase noise was also calculated for the proposed circuit. The phase noise is -114dBc/Hz @1MHz at 1.1 GHz central frequency which is shown in Fig. 7. The dependence of power consumption with center frequency is shown in Fig. 8 where it consumes 23.2 mW DC power from 1.8 V supply at 1.0 GHz frequency. The comparison of the performances of the proposed DCO with other published DCOs on the similar technology was illustrated in Table 2 where the proposed DCO has least power consumption of the same technologies.

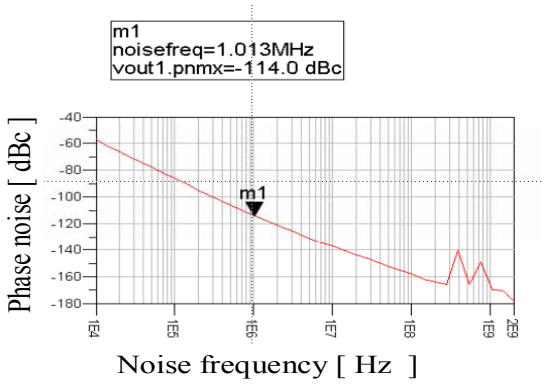

Fig. 7. Simulated phase noise of the proposed DCO for 1.1 GHz central frequency.

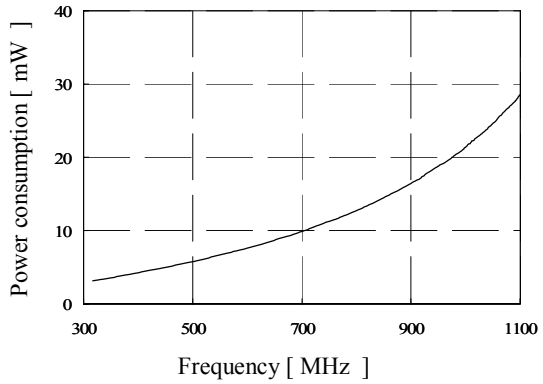

Fig. 8. Dependence of power consumption on central frequency.

Table 2: Comparison of power consumption of the proposed DCO with other published works.

Items / Function	Proposed	Ref [8]	Ref [9]	Ref [10]
Process	0.18µm @1.8V	0.25µm @2.0V	0.18µm @2.0V	0.35µm @3.3V
Output frequency	316-1165 (MHz)	285-1270 (MHz)	100 -3500 (MHz)	45 - 450 (MHz)
Power consumption	23.18mW @1GHz	10mW@ 1.27GHz	NA	100mW@ 450MHz
Phase noise	-114.6 dBc/Hz	-104.4 dBc/Hz	-106 dBc/Hz	NA
Figure of Merit	-159.7 dBc/Hz	-156.4 dBc/Hz	-153 dBc/Hz	NA

V. CONCLUSION

A high-linearity 8-bit digitally-controlled oscillator (DCO) is designed on a ring topology using TSMC 0.18 um CMOS process parameters. One of the advantages of the ring topology over a LC-tank oscillator is that it does not contain any spiral inductor so that the chip size is very small. It consumes 23.2mW power at 1.8 V supply voltage and simulated phase noise is -114dBc/Hz (@1MHz). Verification of the simulated results using the measurement on fabricated chip is necessary which is taken as one of the most important task in near future.

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