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LETTER

Design of 5 GHz-Band Power Amplifier with On-Chip Matching Circuits Using CPW Impedance (*K*) Inverters

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SUMMARY This Letter employs transmission-line theory for the impedance-matching circuits for a single-chip power amplifier (PA) and verifies for 5 GHz-band wireless LAN (IEEE 802.11a) applications. The presented matching circuits are composed of conductor-backed coplanar waveguide (CPW) meander-line resonators and impedance (*K*) inverters. One of the advantages of the presented circuits is that it can save on-chip space occupied by the matching circuits compared to that using the spiral inductors, thus reducing the cost. The prototype chip, which consists of PA and matching circuits, is designed employing the presented theory and fabricated. A few of the measured results to verify the design theory are presented.

key words: *on-chip CPW impedance-matching circuit, 5GHz-band wireless LAN, λ/4 resonator, power amplifier*

1. Introduction

In the RF section of LSI chip, impedance-matching circuits are necessary for interconnecting each part such as low-noise amplifier (LNA), power amplifier (PA), duplexer, mixers, antenna and so on, and lumped elements are usually used for the design of matching circuits. Impedance matching is usually realized by either off-chip bonding wires or on-chip spiral inductors [1]. Realization of matching circuits using the off-chip bonding wires usually demands a trial and error process. On the other hand, conventional matching circuits realized by spiral inductors occupies large on-chip space and it also encounters self-resonance in microwave frequency band which permits its use beyond that frequency. Furthermore, they also suffer from the low quality factor (Q).

Distributed elements made of transmission lines to replace spiral inductors are particularly effective when their size becomes smaller, as the frequency in use increases. Among the transmission lines, coplanar waveguide (CPW) is easy to fabricate by the LSI technology compared to its counter part such as microstrip or strip lines because the signal line and ground plane exist on the same plane [2] so that no via holes are required for integrating active components such as CMOS or BJT on Si-substrate [3].

The applications of the distributed elements made of transmission lines were reported in the CMOS or BiCMOS RF-LSI chip [4]–[9]. The CPW was exploited as an inductor and used to design a conventional-type matching circuit for an LNA [4] in microwave-band frequency, and they were also used as an inductor in monolithic microwave integrated circuit (MMIC) for millimeter-wave devices [5]. However, the application of CPW as an inductor takes larger space than a conventional spiral inductor. Some of the present authors have also implemented the CPW impedance-matching circuits for LNA at 2.4 GHz applications [6]–[9]. In Ref. [6], the performance of off-chip high Tc superconducting CPW to design matching circuit was studied and that employing copper on Si substrate has been studied theoretically [7] and verified experimentally by BiCMOS technology for 2.4 GHz-band applications [8], [9]. As the performance of copper CPW on Si-substrate is highly frequency-dependent, the theory for matching circuits needs to be verified at higher frequencies for universal frequency applications.

In this Letter, the design theory of on-chip impedance-matching circuit using microwave BPF design rules [6]–[9] is employed to design a 5 GHz-band PA for wireless LAN applications (IEEE 802.11a). The designed chip is fabricated and verified using TSMC 0.35 μm one-poly three-metal SiGe BiCMOS technology. The selection of this technology is solely based on the economical and academic interest, and in addition, the model provided for transistors have satisfactory accuracy for RF modeling.

2. Design Theory for On-Chip Impedance-Matching Circuit Using CPW

The design employed here is basically the same as presented in Refs. [7]–[9], therefore only summarized here briefly. The matching circuits consist of impedance (*K*)-inverters and a distributed resonator to realize on-chip impedance matching circuits, and based on the theory of the *n*-pole Chebyshev bandpass filter (BPF) [10].

Figure 1 shows the schematics of the matching circuit and input impedances at the point of *P*, *R* and *S*. Y_L (= $G_L + jB_L$) is the input admittance of PA and $\Delta\ell$ is the line length in order to compensate the jB_L to be zero. Z_1 and $K_{0,1}$ are the characteristic impedance of the quarter wavelength line and *K*-inverter, respectively. The design parameters are given by [10],

$$\Delta\ell = -\frac{B_L}{\omega_0 C_i},$$

$$Z_1 = \frac{\pi}{4}\frac{w}{g_1 g_2 G_L},$$

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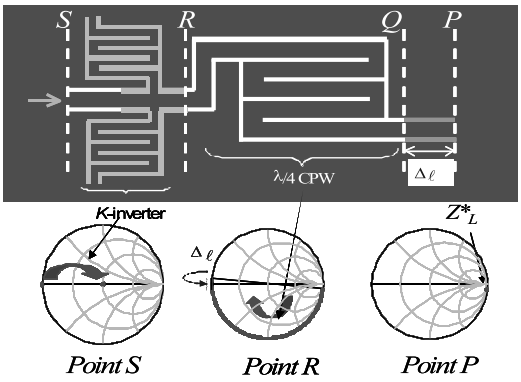


Fig. 1 Schematic of matching circuits employing using $\lambda/4$ line and K-inverter and its representation in Smith chart.

$$K_{0,1} = \sqrt{w}\sqrt{\frac{Z_0 x_1}{g_0 g_1}}, \quad \left(x_1 = \frac{\pi}{4} Z_1\right), \tag{1}$$

where, C_i is the capacitance per unit length (F/m) of the transmission line, and w and g_i are the normalized bandwidth and normalized filter element, respectively [10]. The detail of the derivation of the formulae for g-elements and their numerical values can be found in Ref. [10]. The reactance slope parameter (x_1) is for the series resonance circuit. The design parameters of the CPW matching circuit are f_0 = 5.2 GHz and w = 2% (100 MHz), which is used as an IEEE 802.11a application.

The Smith chart interpretation for matching theory is illustrated in Fig. 1 (lower portion) where $Z^*{}_L$ is the conjugate of input impedance of the amplifier ($Z_L = 1/Y_L = 1/(G_L + jB_L)$) and its position is represented by Point P in Smith chart. The insertion of the $\lambda/4$-transmission line converts the high impedance to very low, and its position is represented by Point R in the Smith chart (see middle of Fig. 1). By using negative capacitance ($-C$), now its position will be shifted to new position so that jB_L becomes 0. Please note that the compensation circuit to achieve $-C$ is realized by adjusting the length ($\Delta\ell$) of the transmission line shorter from $\lambda/4$ so that net length of the transmission line becomes ($\lambda/4 - \Delta\ell$). After jB_L becomes 0, 50 Ω-matching can be obtained by employing the K-inverter (See Point S of Fig. 1).

3. Design of PA with CPW On-Chip Matching Circuits

We use TSMC 0.35 μm BiCMOS process which has 1-poly and 3-metal structure and the thickness of the top metal is 3.1 μm. The conductance of the metal and ε_r of the SiO_2 are 4.1×10^7 S/m and 4.1, respectively. The upper layer is covered by Silicon Nitride whose relative permittivity is 7.9. For size reduction of the matching circuits, the $\lambda/4$ line (line length = 5.8 mm) is bent into meander structure where the width of the signal line and the gap between signal line and ground plane are 5 μm each. The loss due to the meander structure was experimentally evaluated to be 2.5 dB at 5 GHz band frequency [9]. The details of these parameters and their modeling method in electromagnetic simulation are explained in Ref. [9].

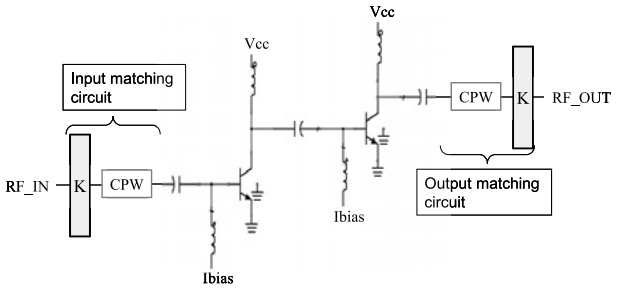


Fig. 2 Circuit model of designed power amplifier (PA).

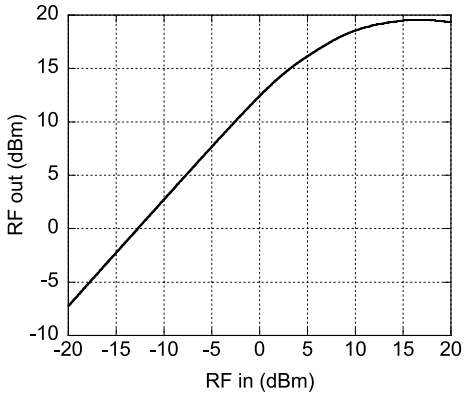


Fig. 3 Input power dependence of the output power of PA.

Figure 2 shows the schematics of the 5.2 GHz-band amplifiers with input and output matching circuit designed by the presented theory. The designed input and output return losses are less than −30 dB at 5.2 GHz, respectively. The current consumption of PA is 59.1 mA. The max gain of PA is 12.1 dB at 5.2 GHz. The noise figures of PA is 5 dB, and these designed parameters satisfy the requirement of wireless LAN (IEEE 802.11a) standard. Figure 3 shows the input power dependence of the output power. The 1-dB compression point is P_{in} = 3.3 dBm. The operating voltage (V_{dd}) of this process is supposed to be 3.3 V.

4. Fabricated Chip and Measured Results

The designed PA with input and output impedance matching circuits is fabricated, and its chip photo is shown in Fig. 4. The input and output pads have coplanar configurations of 100 μm square size whose characteristic impedances are 50 Ω. Spiral inductors are used to supply DC power (bias current) into the transistors. The size of the PA chip including the proposed matching circuit, coplanar probes, and spiral inductors that used to feed bias and DC supply to the transistors is 2.38 mm × 1.05 mm.

The microwave characteristics are measured by using air coplanar probe (Cascade Microtech, GSG150) and vector network analyzer (HP, HP8722C). During fabrication of CPW, we covered the lowest metal in all area of the CPW

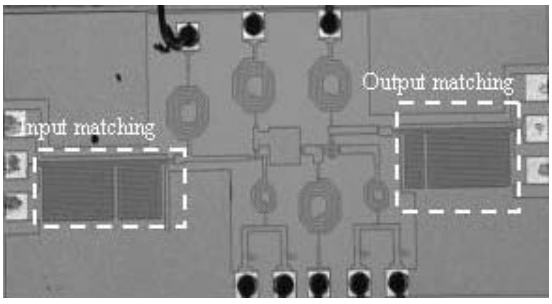


Fig. 4 Microphotograph of PA with the proposed impedance-matching circuits fabricated in TSMC 0.35 μm SiGe BiCMOS 1-poly 3-metal process. (Chip size: 2.38 mm × 1.05 mm).

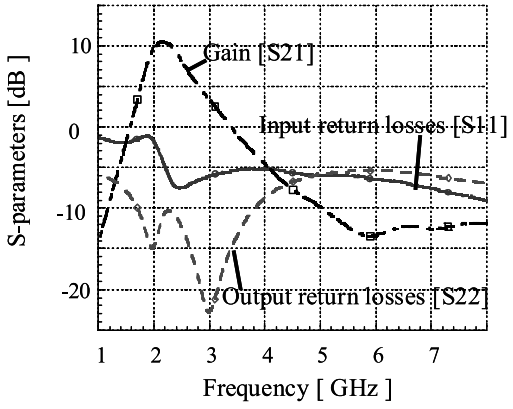
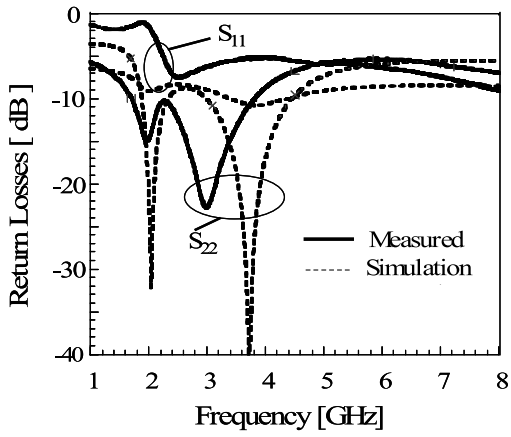
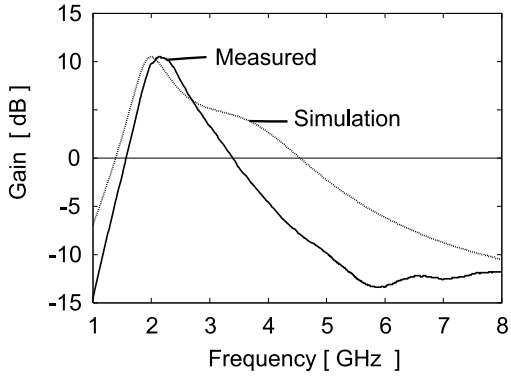


Fig. 5 Measured gain (S_{21}) including input return losses (S_{11}) and output return losses (S_{22}) of the designed PA.



(a) Comparison of input return loss (S_{11}) and output return loss (S_{22}).



(b) Comparison of gain.

Fig. 6 Comparison of S-parameters taking account of inductance of bonding wires from the ground pads.

structure, namely conductor backed CPW in order to avoid the loss in the Si-substrate. Figure 5 shows the measured S-parameters of the PA including gain (S_{21}), input and output return losses (S_{11} and S_{22}), respectively. The measured gain is obtained about 10 dB at frequency of 2.2 GHz although its designed value is 12.1 dB at 5.2 GHz. The discrepancy in the measured and designed frequency is caused by the parasitic inductance of the bonding wires that connects the grounding pad which was not considered during the design. Taking account of this inductance in simulation, Fig. 6 shows the comparison of the simulated results of S-parameters. In Fig. 6(a), comparison of input return loss and output return loss are shown and comparison of gain is shown in Fig. 6(b), where the simulated results including gain are very close to the measured results. This ensures that the presented method can be employed in order to design the on-chip impedance-matching circuit using $\lambda/4$ CPW and K-inverters at 5 GHz band wireless applications.

The size of the matching circuit occupied in Fig. 4 is 530 μm × 275 μm. For size comparison, the matching circuits of the same PA were also designed using spiral inductors where the size was 540 μm × 718 μm. Thus, the matching circuit designed by the presented theory saves about 40% in chip size. This ratio was about 30% at 2.4 GHz band [9]. Thus it is inferred that, if the operating frequency increases, this ratio becomes more effective.

5. Conclusions

We designed the single chip SiGe BiCMOS Power amplifier with matching circuits for wireless LAN (IEEE802.11a) applications, which are composed of quarter-wavelength resonators and K-inverters using CPW. The CPW are realized by meander structures so that they can be fabricated inside a chip and their shape can be adjusted in order to exploit the vacant space on the Si-substrate effectively. A comparison shows that the matching circuit designed by the proposed method saves about 40% of the chip space of that when using the spiral inductors. This ratio was about 30% when designed for 2.4 GHz applications [9].

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References

[1] T.H. Lee, H. Samavati, and H.R. Rategh, "5-GHz CMOS wireless LANs," IEEE. Trans. Microw. Theory Tech., vol.50, no.1, pp.268–280, Jan. 2002.

[2] I. Wolff, Coplanar microwave integrated circuits, Wiley Interscience, 2006.

[3] I. Toyoda, "Circuit design using coplanar waveguides," Microwave Workshops and Exhibitions (MWE'96) Digest, pp.461–469, 1996.

[4] M. Ono, N. Suematsu, S. Kubo, K. Nakajima, Y. Iyama, and O. Ishida, "Si substrate resistivity design for on-chip matching circuit based on electro-magnetic simulation," IEICE Trans. Electron., vol.E84-C, no.7, pp.923–930, July 2001.

[5] Y. Umeda, T. Enoki, and Y. Ishii, "Sensitivity analysis of 50-GHz MMIC-LNA on gate recess depth with InAlAs/InGaAs/InP HEMTs," IEEE MTT-S Int. Microw. Symp. Dig., pp.123–126, 1994.

[6] H. Kanaya, Y. Koga, J. Fujiyama, G. Urakawa, and K. Yoshida, "Design and performance of high Tc superconducting coplanar waveguide matching circuit for RF-CMOS LNA," IEICE Trans. Electron., vol.E86-C, no.1, pp.37–41, Jan. 2003.

[7] H. Kanaya, T. Nakamura, K. Kawakami, and K. Yoshida, "Design of coplanar waveguide matching circuits for RF CMOS front end," IEICE Trans. Electron. (Japanese Edition), vol.J87-C, no.12, pp.1017–1023, Dec. 2004.

[8] H. Kanaya, R.K. Pokharel, F. Koga, Z. Arima, S. Kim, and K. Yoshida, "Design of coplanar waveguide on-chip impedance-matching circuit for wireless receiver front-end," 2006 IEEE IMS/RFIC Symposium, paper no.1229, San Franscisco, USA, June 2006.

[9] H. Kanaya, R.K. Pokharel, F. Koga, and K. Yoshida, "Design and verification of on-chip impedance matching circuit using transmission line theory for 2.4 GHz band wireless receiver front-end," IEICE Trans. Electron., vol.E89-C, no.12, pp.1888–1895, Dec. 2006.

[10] G.L. Matthaei, L. Young, and E.M.T. Jones, Microwave Filters, Impedance-Matching Networks, and Coupling Structures, Artech House, Norwood, MA, 1980.