Design of VCO Using On-Chip CPW Resonator for 5 GHz-Band Wireless Applications

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Introduction

Distributed transmission line resonators have become the interest of research subjects recently [1]-[4] because of their size which becomes more compact, as the frequency of application increases. Among the various transmission lines, coplanar waveguide (CPW) has more engineering applications because it is easy to fabricate by LSI technology since the signal line and ground plane exist on the same plane so that no via holes are required for integrating active components such as transistors on Si-substrate.

The applications of the CPW were reported for on-chip LSI applications. The CPW was exploited as an inductor and used to design a conventional-type matching circuit for LNA [2] in microwave-band frequency, and they are most popular in monolithic microwave integrated circuit (MMIC) [3]. However, the application of CPW lines as an inductor takes larger space than the conventional spiral inductors [2]. Some of the present authors have also implemented the on-chip CPW impedance-matching circuit for a 2.4 GHz RF front end using impedance inverters [4].

In this paper, transmission characteristics of the on-chip meander CPW resonator fabricated in TSMC 0.18um CMOS process is first investigated experimentally and an equivalent circuit is developed. Later, we implemented on-chip CPW resonator to design a VCO for 5GHz-band wireless applications. One of the advantages of the proposed VCO using on-chip CPW resonator in comparison to a LC-VCO is the chip area which is reduced by about 30, and higher frequency-tuning range (FTR).

Design of On-Chip CPW Resonator

The on-chip meander CPW resonator is designed, fabricated, and measured. An equivalent circuit is developed to reproduce the experimental results whose model parameters are useful to extract RCX (Resistance-Capacitance extraction) of the whole chip of the proposed VCO. Fig. 1 shows the chip photo of dummy pads and interconnects (Fig. 1(a)), and on-chip meander CPW (Fig. 1(b)). In order to avoid the loss in the Si-substrate, we covered the lowest metal (metal-1) in all areas, namely conductor backed CPW. The signal width and the interval between the slots of the CPW transmission line are 5?m and 5?m, respectively. In order to de-embed he measured raw data, at first, we measure S-parameters of total (Fig. 1(b)) and open dummy chip (Fig. 1(a)), respectively. Next, S-parameters are transformed into Y-parameters using Equation (1), then converted to Z-parameters in order to compare the results between simulation using the Equivalent circuit of Fig. 2 and measurement.

$$[Y]_{\mathrm{TML}} = [Y]_{\mathrm{total}} - [Y]_{\mathrm{dummy}} \qquad (1)$$

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Finally, the transformed results are compared in Fig. 3 using simulation and measurement, where the measured results are well reproduced by the simulation using the equivalent circuits. It is thus inferred that the equivalent circuits developed in Fig. 2 can be used to carry out post-layout simulation of the whole chip.

Design of VCO Using On-chip CPW Resonator

In this section, we design two 5GHz-band VCOs comparatively; the first one employing on-chip CPW resonator and the latter one employing the LC-tank resonator. Fig. 4 shows the schematics of these two VCOs. In Fig. 4(a), LC-VCO is shown where widely used CMOS cross-coupled structure [5] [6] is used, and that of using the CPW resonator is shown in Fig. 4(b). Co-simulations in Agilent ADS are used to simulate the passive components together with active elements. Total length of on-chip meander CPW is 3300μm which is to be a quarter-wavelength resonator for 5.2GHz frequency.

Fig. 5 shows the post-layout simulated output voltage waveforms of the designed VCOs. Fig. 6 shows the chip photo of fabricated VCO employing CPW resonator and Fig. 7 shows its one of the measured spectrum. In Fig. 5, maximum peak voltage of LC-VCO is greater than that of the VCO using on-chip CPW resonator and this is clearly reflected in the performance of the phase noise of the VCO in Table 1. However, from the table, other performances such as FTR (Frequency tuning range) and chip size of VCO using CPW resonator has better performance than LC VCO.

Conclusion

A 5GHz-band VCO employing on-chip CPW resonator instead of LC-tank resonator is proposed, designed and fabricated on TSMC 0.18μm CMOS technology. The advantages of employing CPW resonator is the wide frequency-tuning range, and it also saves about 30% of chip size. The simulated noise figure of the proposed VCO employing on-chip CPW resonator slightly worsen than that of LC VCO.

Acknowledgment

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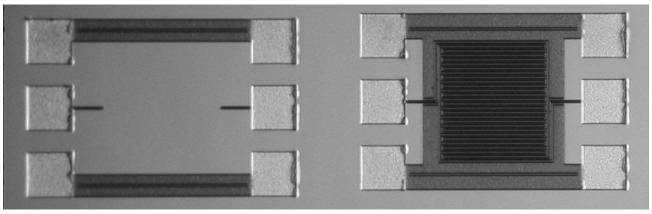
Figures



(a) Dummy chip (b) On-chip CPW meander line

Figure 1. Chip photo of fabricated CPW meander line.

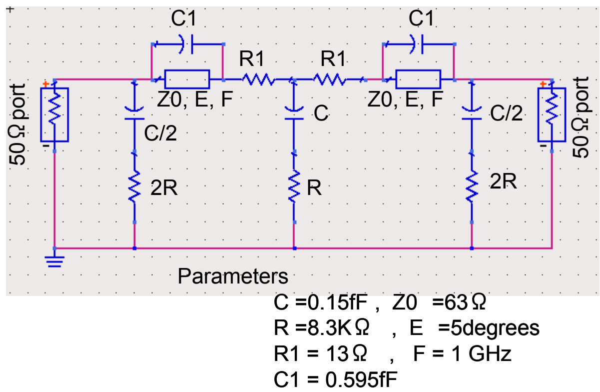
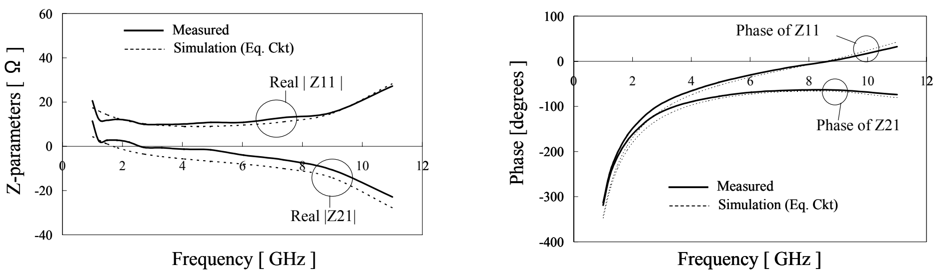
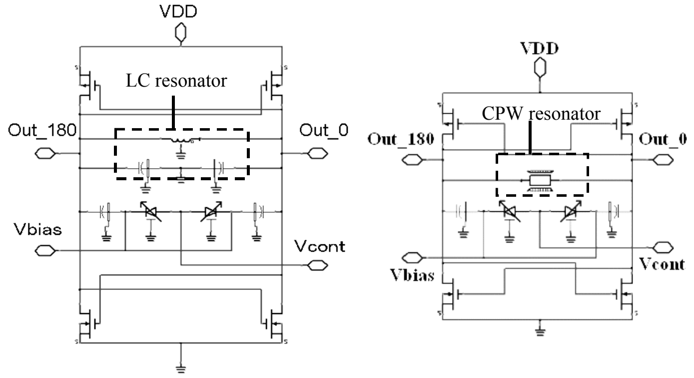


Figure 2. Equivalent circuit of on-chip CPW meander line.



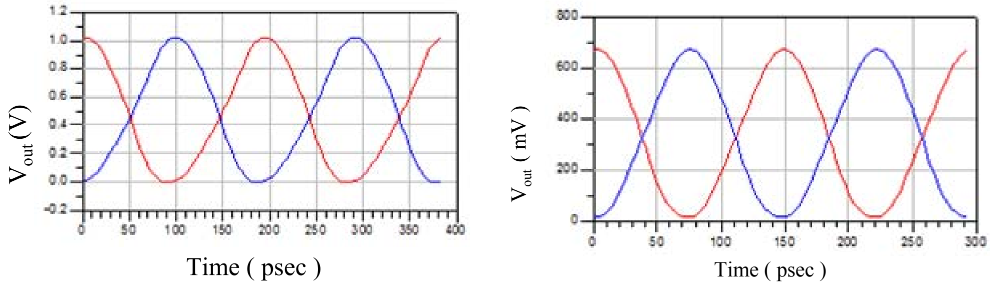
(a)Real part of Z-parameters (b) Phase of Z-parameters

Figure 3. Comparison of simulated Z-parameters using equivalent circuit with the measured results.



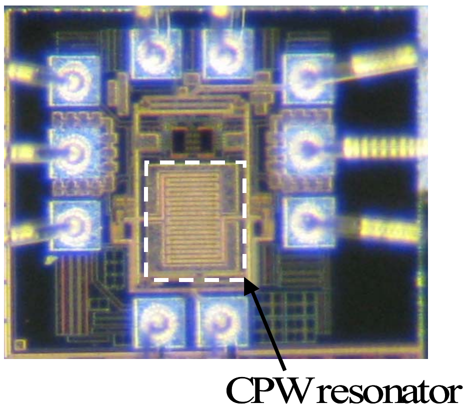
(a) LC VCO (b) VCO using CPW resonator

Figure 4. Schematics of VCO using LC resonator and CPW resonator.



(a) Of LC VCO. (b) of VCO using on-chip CPW resonator.

Figure 5.Output voltage waveforms of designed VCOs.



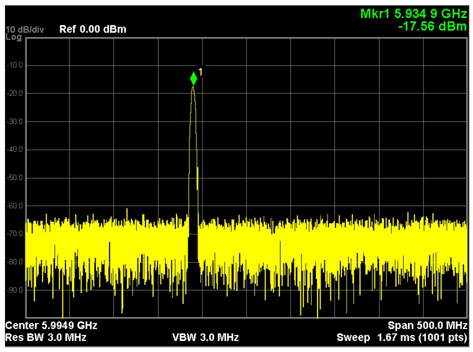


Fig. 6. Chip photo of VCO using CPW resonator. Fig. 7. Measured spectrum.

TABLE I. COMPARISON OF SIMULATED PARAMETERS BETWEEN TWO VCO USING LC RESONATOR AND ON-CHIP CPW RESONATOR, RESPECTIVELY. [FTR=FREQUENCY-TUNING RANGE]

	LC resonator	CPW resonator
Center Frequency [GHz]	5.2	5.9
FTR [%]	7	10.2
Phase noise [dBc/Hz]@1MHz	-118	-109
Area [m^2]	$1.4x10^{-7}$	$1.01x10^{-7}$