Design of Digitally Controlled LC Oscillator with Wide Tuning Range in 0.18um TSMC CMOS Technology

Abhishek Tomar, Ramesh Pokharel, Haruichi Kanaya, Keiji Yoshida
Department of Electronics, Graduate School of Information Science and Electrical Engineering, Kyushu University, Japan
Email:tomar@yossvr3.ed.kyushu-u.ac.jp

Introduction

The explosive growth of wireless mobile systems in GHz range has forced the implementation of radio frequency integrated circuit in low cost CMOS technology. Scaling of the CMOS technology and reduction in supply voltage complicates the implementation of RF circuits in CMOS technology and favor the use of digital control approach for RF circuit. [1]. The Oscillator being a critical component of the wireless system is necessary to be implemented and integrated with the complete system on the same chip further favors digital implementation.

Recently, many digitally controlled oscillators are implemented [2-5]. The DCO described in [3] is implemented in ring oscillator structure, which gives poor phase noise performance with low operating frequency and is not suitable for GHz applications. The LC type DCO [4,5] provides good phase noise but high frequency resolution, is achieved with small size capacitors and this has used most advanced and expensive technology. Now, tuning range of the DCO is also important for the implementation of multiple standards and wide band circuits on the same chip.

In this paper, we present the design of LC-DCO with low phase noise and low power dissipation. Particular attention is given to achieve the wide tuning range. A varactor array is implemented using new logic, which made the significant reduction in the number of signal lines and the reduction in the size of local decoder, used to decode the input control word. This decoding scheme reduces the size of parasitic capacitance and power dissipation and provides wide tuning range of the proposed DCO.

LC DCO

The proposed structure of LC-DCO is shown in Fig.1. The inductance L and capacitor array C makes the resonance circuit. The frequency of oscillation can be given by equation

$$f = \frac{1}{2\pi\sqrt{LC}}$$

The frequency of DCO is changed with voltage-controlled varactors that can be easily implemented. The parasitic resistance of inductance and capacitor bank array is compensated by the cross coupled structure of NMOS transistor.

The tank and active circuit of the proposed DCO are optimized for the low power consumption and low phase noise. From ref [6], it is clear that maximal L/R and L/C ratio is needed to optimize LC tank. The differential coil type inductance provided by 0.18um TSMC is used in the tank, to take the advantage of coupling effect in differential coil that increases the effective inductance and improves the quality factor. PMOS transistors are used as

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varactors. For large tuning range, the higher value of Cmax/Cmin with minimum area is selected. The dimension of PMOS for the varactor is W=220nm and L=500nm. The length of the transistor used is also more than minimum length (180nm) of technology to decrease the effect of the source and drain overlapping capacitance. To realize the active part, only two cross-coupled NMOS transistors are used. Current source eliminated to maximize the output swing and elimination of important source of phase noise.

A varactor array is used to control the output frequency of DCO. The main problem associated with frequency control is the significant value of parasitic capacitance at output node that limits the tuning capabilities and increases the power dissipation. Therefore, this varactor array is optimized for reduction in parasitic capacitance. In the ref [2], for the 10 bit DCO varactor array is designed by using two types of cells: type 1 has 4 pairs of PMOS varactors in parallel and type 2 used single pair of PMOS varactors, for higher order 8 bit and lower order 2 bit respectively. This has reduced the signal lines to 48 for 16*16 cells varactor array and reduces the area by 25%.

In this proposed DCO for the higher order 8 control bits (D2-D9), we also use type 1 varactors. The new logic-decoding scheme is proposed in which thermometer coding is used at alternate switching position and in between this alternate switching two rows simultaneously flip its signal. The proposed scheme is demonstrated in Table1 with the help of only two control inputs. The total number of control lines required is reduced to 32 instead of 48. Also, it helped in reducing the size of local decoder. Thus, more than 40% reduction in varactor array area is achieved. Column decoder in this scheme also used thermometer coding. The lower two bits (D1-D0) are used to get minimum size resolution and used binary coding. Two different types of varactor cells shown in Fig.2 are used the serpentine way of switching for improved matching.

Table1: Demonstration of switching of cells in varactor array

Control word D7 D6	**Row decoder Output** R1	R2	R3	R4	**Varactor cells in** (Here C represents the column code)
00	1	0	1	1	Row 1, will turn ON for C=1, otherwise OFF Row 2, Row3, Row4 all will be turn OFF
01	0	1	1	1	Row 1, will turn ON. Row 2, will turn ON. For C=0, otherwise OFF Row 3, Row 4 all will be turn OFF
10	0	0	1	0	Row 1, Row2 will turn ON. Row 3 will turn ON. For C=1,otherwise OFF Row 4 all will be turn OFF
11	0	0	0	1	Row 1, Row2, Row 3 will turn ON. Row 4 will turn ON. For C=0, otherwise OFF

Simulation Result

The proposed DCO was designed in TSMC 0.18um CMOS technology. The tuning range achieved is 5.13GHz to 7.06 GHz. The core of oscillator consumes 4.25mA of current @ 0.8 V power supply. The simulated phase noise is –120dBc/Hz @1MHz offset at the center frequency of 5.4GHz. This is shown in figure 4. In Table 2, DCO is compared with other published DCO, which shows the significant improvement in tuning range.

Table2: Comparison of various existing DCO

DCO	Technology [*nm*]	Tuning range [*MHz*]	Frequency [*GHz*]	Phase noise [*dBc/Hz*]	Current [*mA*]
[2]	130	500	2.4	-112@500kHz	2.3
[4]	65	1030	10	-102@1MHz	3
[5]	90	900	2.4	-165@20MHz	18
This	180	2000	5.5	-120@1MHz	4.25

Conclusions

A low power, low phase noise and wide tuning range of fully integrated LC-DCO is designed in 0.18um CMOS technology. The proposed scheme for varactor cell has reduced the parasitics capacitance and 35% tuning range is achieved.

Acknowledgements

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Figures

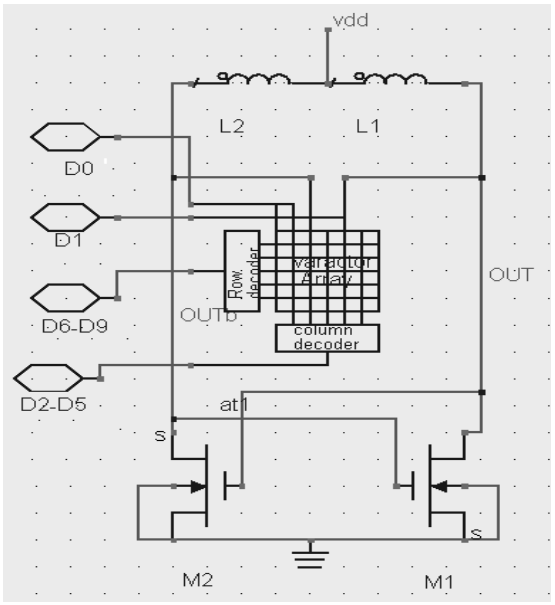


Fig.1. Block diagram of proposed DCO.

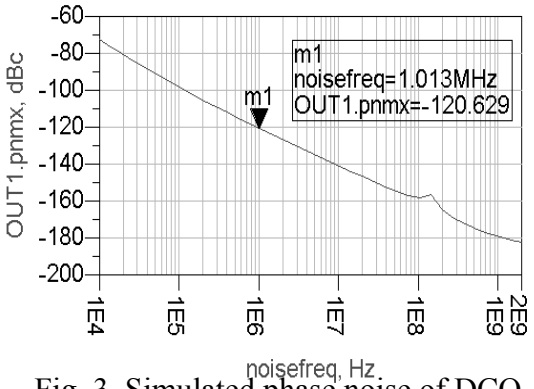


Fig. 3. Simulated phase noise of DCO at 5GHz frequency.

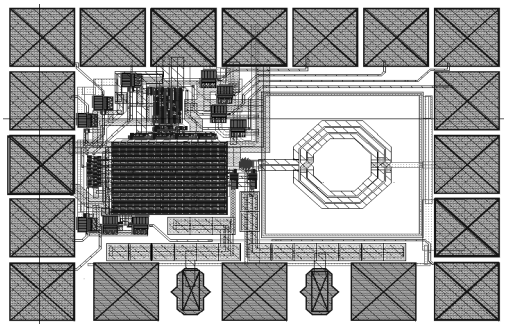
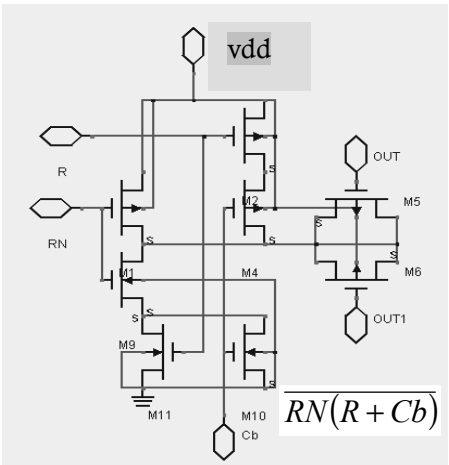


Fig.4. Layout of the proposed DCO.



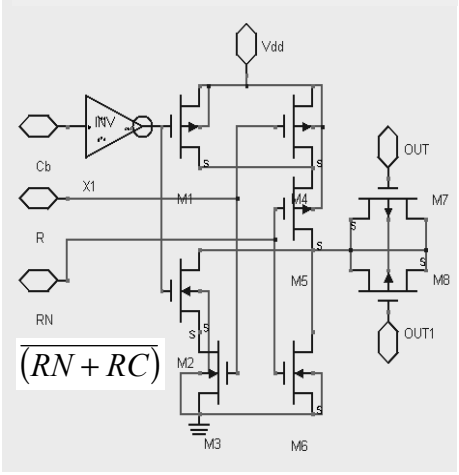


Fig.2. Schematic of varactor cell for odd (above) and even (below).