# Comparison between Bipolar and NMOS Transistors in Linearization Technique at 5GHz Low Noise Amplifier

A. I. A. Galal, R. K. Pokharel, H. Kanaya, and K. Yoshida
Graduate School of Information Science and Electrical Engineering
Kyushu University, Motooka 744, Nishi-ku, Fukuoka 819-0395, Japan
E-mail: galal@yossvr3.ed.kyushu-u.ac.jp

## Introduction

Low noise amplifier (LNA) is the first stage of a transceiver system, which has the main effects on the performance of signal to the remaining stages. The specification of LNA must be satisfied the following, high gain, low noise figure, good matching, low power consumption, low cost, and also high linearity. LNA designers always adopt two mode design strategy to achieve all of the above goals, one is high gain, low noise, but low linearity for small desired signal with small interference and another is low gain, high linearity but high noise for large desired signal with large interference [1]. Theoretically, the responsible of third-order nonlinearity in MOSFET transistor is the third-order derivative of dc transfer characteristic, changes from positive to be negative in the moderate inversion region [2]. Several techniques are used to achieve highly linearity LNA depend on how to cancel the third-order derivative. The feed-forward technique is the common topology to get high linearity, and it used in different forms. In [3] the output is taken as the difference of two amplifiers whose inputs are scaled to obtain zero third-order distortion. The other type is used for amplifiers, one biased in strong inversion, and the other biased at weak inversion, the negative peak of a third-order derivative of the first amplifier is canceled by the positive peak of the second amplifier. The negative feedback technique also is popularly adopted to improve linearity, but it cannot be easily performed at RF frequency due to stability consideration. The basic idea of linearization is to use additional transistor's nonlinearity to compensate or cancel the nonlinearity of a main operation device. The conventional way involves MOS transistors working in triode or weak inversion to provide linearization. Bipolar is available in CMOS technology, it is sufficient to be in linearization [4]. In this paper, a linearization technique is derived from multi-gated linearization by using bipolar transistor and also by using NMOS transistor. Comparison between two cases is presented at the end of this paper.

## Linearization technique

The nonlinearity of a MOS transistor arises from its voltage to current characteristic, which can be described with the power series as following:

$$I_D = G_{m1}V_{gs} + G_{m2}V_{gs}^2 + G_{m3}V_{gs}^3 + \ldots\ldots \qquad (1)$$

Where $G_{m1}$ is the main trans-conductance, $G_{m2}$ represents its second nonlinearity obtained by the second-order derivative, and $G_{m3}$ is the third –order derivative. The input third-order intercept point of a nonlinear device is:

978-1-4244-2642-3/08/$25.00 ©2008 IEEE

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{G_{m1}}{G_{m3}}\right|} \qquad (2)$$

The value of IIP3 is maximum if the value of $G_{m3}$ is minimum. Our goal is how to minimize the value of $G_{m3}$ to provide high linearity.

## Circuit design

The proposed LNA is shown in Fig. 1 it consists of the main NMOS transistor M1, and an auxiliary bipolar transistor M2. Source degeneration inductor L2 and input inductor L1 are used to provide the input matching. C1, C2, and C3 are coupling capacitors. Output inductor L3 is used to get output matching at 5GHz. The sizes of M1 and M2 are properly selected, and M1 is biasing in a strong inversion region where its IM3 has negative sign and M2 has been positive signed IP3 to achieve lowest IM3. Fig. 2 shows the post-layout simulation, S11 is -15.9dB, S22 is -15.8dB, the gain is 10.5dB, and noise figure is 2.1dB. Fig. 3 illustrates third input intercept point IIP3 of the implemented high linearity LNA. The LNA shown in fig.1 was fabricated in TSMC 0.18 μm CMOS technology and the microphotograph is shown in Fig. 4. The measurement of IIP3 is presented in Fig. 5 and gives IIP3= 16dBm.

Bipolar transistor is replaced in Fig. 1 by NMOS transistor to compare the linearity by using the different types of transistors. Input and output matching are presented. The third order nonlinearity changes from positive to be negative in the moderate inversion linear so M1 is biased at a strong inversion region and M2 is biased at a weak inversion region. The result of connected the two outputs of M1 and M2 is highly linear amplifier because the third nonlinearity of the first amplifier is canceled by the second amplifier. Fig. 6 presents the S parameters and noise figure of the designed LNA by using NMOS transistor and their values are given in Table 1. The input third order intercept point is 15dBm which means this circuit gives high linearity but when make small changes in the circuit the linearity highly degraded. When change only in a corner case of RF transistor from T/T to S/S the linearity drop to be 6dBm.The main drawback of this technique is that the NMOS transistor is biased at a swept point hence, limiting the transconductance of the input stage and reduced gain and increased noise figure.

## Results analysis and discussion

The FET transistor when biased at the zero crossing point will be highly linear, but the region over which this linearity boost can be obtained is very narrow and the bias point is bound to change due to process variations leading to a very sensitive and limited improvement. When operate the transistor in slow/slow corner case, the results of IIP3 is reduced to less than the half, this means this NMOS is very sensitive to small variation, thus linearization technique using bipolar transistor is quiet good and more stable over the changes.

## Conclusion

This paper presents a comparison between bipolar and NMOS transistor to get high linearity amplifier. Using bipolar transistor, the amplifier has high linearity, and it does not sensitive to

component variations. High linear amplifier using bipolar transistor has been designed and was fabricated using TSMC 0.18um CMOS 1P6M process. Table 1 presents the comparison between this work and other published work. The high linearity amplifier exhibits measurements results as 10.5 dB gain, noise figure less than 2.1 dB, input return loss is less than -15.9 dB, output return loss less than -15.8 dB, input third order intercept point is more than 16dBm, and 7.6 mW of power consumption at 5 GHz.

Table 1. Comparison with other published work

| References | Frequency (GHz) | S11(dB) | S22(dB) | NF(dB) | Gain(dB) | IIP3(dBm) | Technology |
|---|---|---|---|---|---|---|---|
| [5] | 2.4 | -10.1 | -10.5 | 2.9 | 10.1 | **4** | 0.25µmCMOS |
| [6] | 2.6 | -23.3 | -6.8 | 2.95 | 15.2 | **3** | 0.18µmCMOS |
| This work (Bipolar) | 5 | -15.9 | -15.8 | 2.1 | 10.5 | **16** | 0.18µmCMOS |
| This work (NMOS) | 5 | -10 | -14 | 2.2 | 9 | **6** | |


## Acknowledgment

This work was partly supported by a grant of Knowledge Cluster Initiative implemented by Ministry of Education, Culture, Sports, Science and Technology (MEXT), KAKENHI (B), and KIBAN (B). This work was also partly supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with CADENCE Corporation and Agilent Corporation.


## References


[1] M. Lin, Y. Li, and H. Chen, "A novel IP3 boosting technique using feedforward distortion cancellation method for 5 GHz CMOS LNA," IEEE Radio frequency integrated circuits symposium, pp. 699-702, June 2003.

[2] S. Ganesan, E. S. Sinencio, and J. S. Martinez, "A highly linear low noise amplifier," IEEE Transaction on microwave theory and techniques, vol. 54, no. 12, Dec. 2006.

[3] Y. Ding, and R. Harjani, "A +18dBm IIP3 LNA in 0.35µm CMOS," IEEE International solid state circuits conference, San Francisco, CA, pp. 162-163 Feb. 2001.

[4] C. Xin, and E. S. Sinencio , "A linearization technique for RF low noise amplifier," IEEE ISCAS, pp. 313-316, vol. 4, May 2004.

[5] V. Aparin, G. Brown, and L. E. Larson, "Linearization of CMOS LNA' S via optimum gate biasing," IEEE Int. Circuits System Symp., Vancouver, BC, Canada, vol. IV, pp.748-751, May 2004.

[6] H. Y. Liao, Y. T. Lu, J. D. Deng, and H. K. CHiou, " Feed-forward correction technique for a high linearity WiMAX differential low noise amplifier," RFIT2007-IEEE, Int. workshop on radio frequency integration technology, pp. 218-221, Dec. 2007.

## Figures

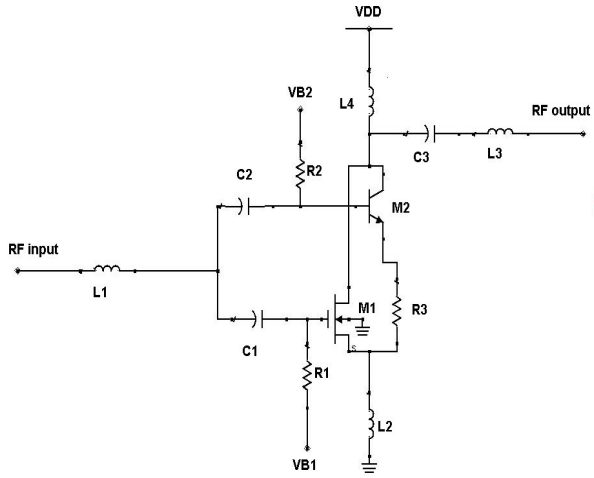


Figure 1. LNA using bipolar transistor.

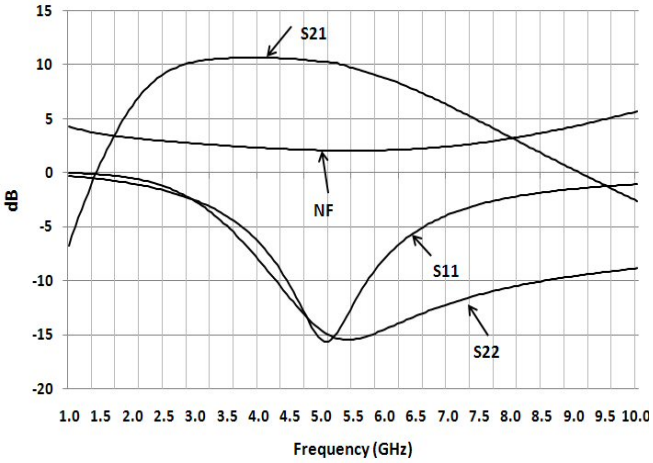


Figure 2. S parameter and noise figure using bipolar

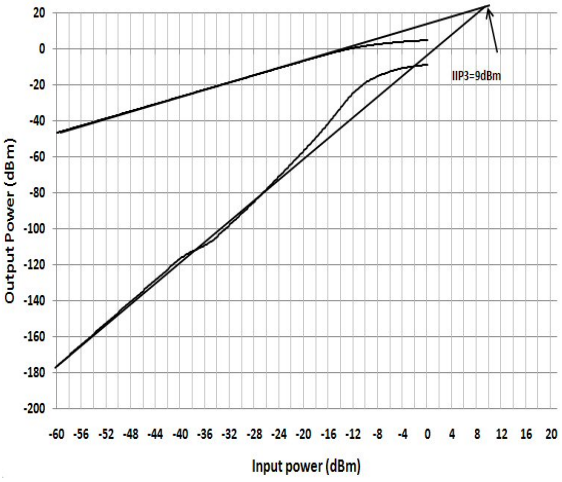


Figure 3. Simulated IIP3.

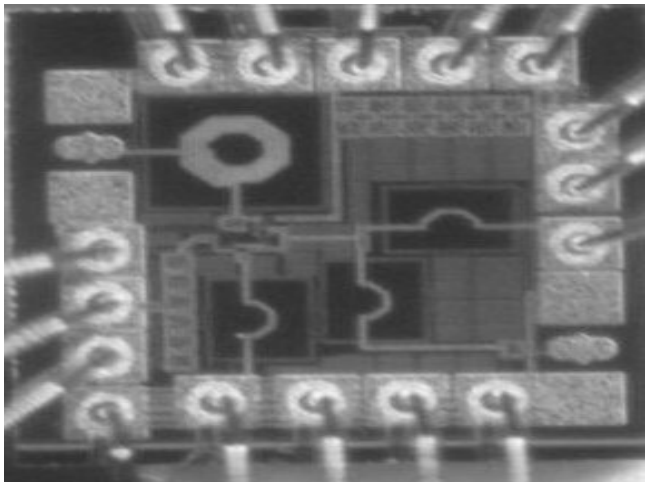

Figure 4. Microphotograph of LNA.

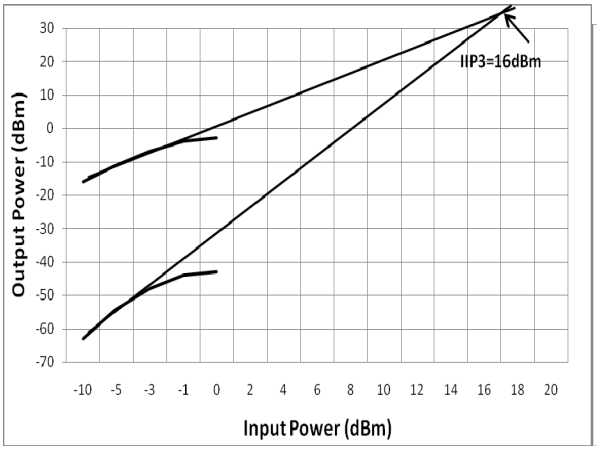


Figure 5.Measured of IIP3.

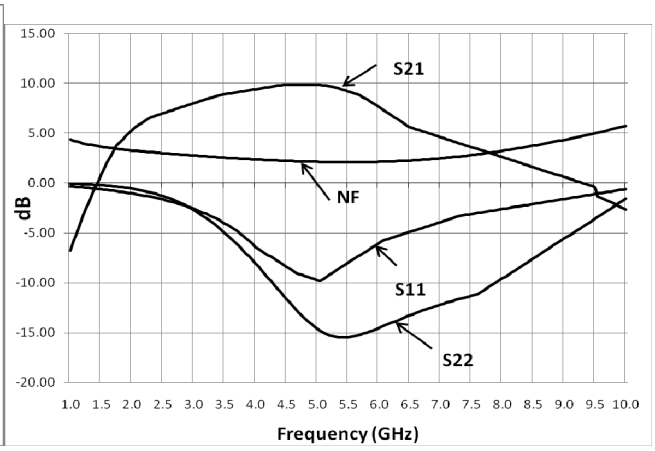


Figure 6. S parameters and noise figure using NMOS.