Low Noise Wide Tuning Range Quadrature Ring Oscillator for Multi-Standard Transceiver

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Abstract—**This letter presents a low phase noise quadrature ring oscillator with new start-up circuit. The oscillator architecture is a two-stage differential ring with an additional pair of transition-assistance transistors. The circuit was implemented in 0.18 μm CMOS technology and the measured tuning range of the prototype device is from 1.7 GHz to 5.5 GHz and figure of merit (FOM) is -162 dB. The proposed area of application is the core of the local oscillator in a multi-standard wireless transceiver.**

Index Terms—**Local oscillator, multi-standard wireless transceiver, phase noise, quadrature ring oscillator.**

I. INTRODUCTION

RING oscillators have been studied extensively in recent times for high frequency wireless communications [1]–[8] because of their compact size compared to an inductor-capacitor (LC)-tank oscillator. One of the advantages of the ring oscillator is that it does not need an inductor that takes a large on-chip area in silicon substrate and usually degrades the performance of a LC-tank resonator. However, maximal operation frequency of the ring oscillators is limited, and it suffers from high phase noise and high power consumption. One of the known approaches to achieve high oscillation frequency for ring oscillators is usage of current mode logic (CML) delay cells with a tail current source [9]. As one uses shorter gates and lower source to drain voltages, differential resistance of the tail current source become small. Thus CML inverters have insufficient common-mode rejection in deep-submicron CMOS technology, and furthermore, non-ideal tail current source costs in the performance of phase noise and power consumption as the oscillation frequency increases.

An alternative of the CML cell [9] is sub-feedback loops [2]. Theoretically, the sub-feedback design allows an arbitrary number of output taps in oscillator rings while maintaining the oscillation frequency of the fastest three-stage ring oscillator. It eliminates tail current sources altogether and reduces power consumption. Another high-frequency alternative is the inductor-coupled ring oscillator [10], which has the lowest phase noise among ring oscillators, but they are plagued by the large size of the coupling inductors that makes matching of the

transistors in the quadrature ports difficult and the entire oscillator more prone to static phase mismatch as layout distance between oscillator ports is increased.

Furthermore, the quadrature ring oscillator proposed in ref. [3] employed two differential inverters. Although the oscillation frequency is 10 GHz, the tuning range is only 16% of the central frequency. The reason for the reduction in tuning range is small gain of CML inverters and usage of active inductors to boost it, resulting in the narrowband operation. A two-stage differential inverter was also proposed [4] to implement quadrature outputs that has a phase noise of 117 dBc/Hz (@1 MHz offset) at the cost of power dissipation.

In this Letter, a novel architecture for a quadrature ring oscillator is proposed using power efficient inverters, and this successfully solved both problems of high phase noise and low oscillation frequency. The proposed design consists of a digital inverter and an additional pair of transition-assistance transistors where one is an over-sized n-channel and another one is a small p-channel transistor. The proposed design exploits the merit of high tuning range and high oscillation frequency of the oscillators [7] and [8], respectively.

II. DESIGN OF QUADRATURE RING OSCILLATOR

The proposed design employs two-stage differential inverter ring topology, although the circuit topology can be alternatively interpreted as a four-stage single-ended inverter ring with sub-feedback loops index $i = 3$ [2]. The schematic of the proposed oscillator core is shown in Fig. 1 where the wiring detail of inverters (I1-I4) is shown in the upper side and the schematic of an inverter is shown in the lower side. Each inverter consists of four transistors where transistors M1 and M2 makes a digital inverter with the same slew rate on the rising and falling transitions and on the other hand, transistor pairs M3 and M4 are transition-assistance transistors where M3 is an over-sized n-channel transistor and M4 is a small p-channel transistor. If small p-channel transistor M4 of the inverters I1-I4 is removed from the circuit, the resulting circuit will be identical to an assisted-transition inverter [6]. Although the additional PMOS reduces the maximum oscillation frequency by 3%, it suppresses the parasitic differential oscillator mode. In the differential oscillation mode pair of the inverters I1 and I3, the output voltage is close to ground level, while another pair, I2 and I4 has the high voltage level (Vdd) at outputs. This happens because at low voltage in the source nodes of M1, the gain-bandwidth product of the transition-assistance inverter M3, M4 become very small and is unable to respond to gate voltage transition. The size of transistor M4 should be large enough to pull up the voltage at the drain of M3 to MOSFET threshold voltage in the half period of the fastest parasitic oscillation but larger size of M4 decreases
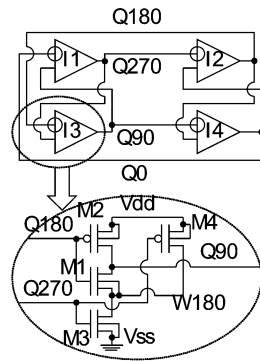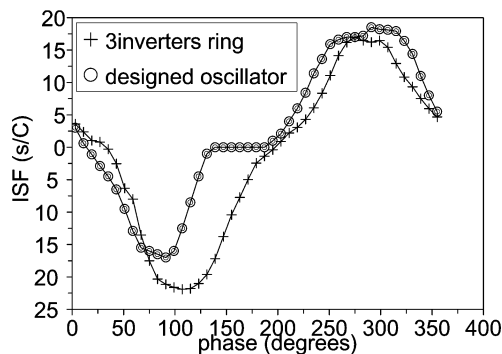
Fig. 1. Schematic of the proposed quadrature ring oscillator core.

Fig. 2. Comparison of simulated ISF between standard three-stage oscillator and the proposed quadrature ring oscillator.

Fig. 3. Photograph of the fabricated chip.

Fig. 4. Measured power consumption during two modes of the proposed quadrature ring oscillator.

the oscillating frequency. The size of M4 is thus traded off to be less than one tenth of the M3 gate width in this design. Therefore, introduction of the M4 effectively solve the two-stage ring oscillator stability problem [6].

One of the factors in reduction of the phase noise in the proposed quadrature ring oscillator is the reduction of the impulse sensitivity function (ISF) [4], defined as conversion coefficient of noise charge (coulombs) to phase deviation (seconds). As one can see from Fig. 2, the designed oscillator, unlike a three-stage ring oscillator, has a near-zero flat ISF region. ISF improvement reduces phase noise by approximately 2 dB. Another factor in phase noise reduction is the thermal noise bandwidth of the oscillator. Since the gate capacitance of inverters act as a low-pass filter for thermal noise, a design with larger gates, while oscillation frequency and power dissipation are fixed, is preferable. In the proposed design, the node capacitance to power dissipation ratio is approximately two times larger than in simple digital inverter, although transition speed is the same. Because of the reduced two times thermal noise bandwidth, the designed oscillator has a further 6 dB phase noise reduction compared to conventional single ended three-stage ring oscillators. Thus, the total reduction in phase noise is 8 dB, so the designed device fills the gap in the FOM between ring oscillators and LC-oscillators.

III. IMPLEMENTATION AND MEASUREMENT

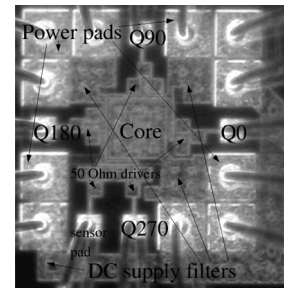Complete design of quadrature VCO was implemented in the TSMC 0.18 μm CMOS technology. Chip photo is shown in
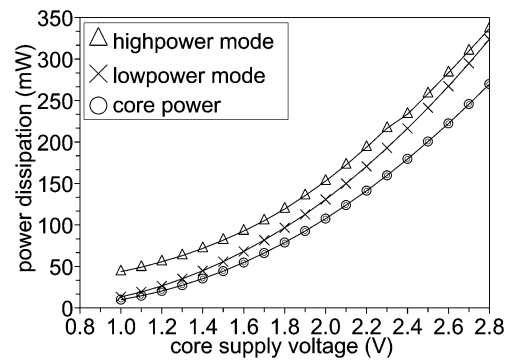
Fig. 3 where the size including bonding pads is 0.30 mm2 and the core area of the oscillator is only 0.01 mm^2. The core area is also limited by the local heating of the crystal. The test for thermal stability of the device was performed where the thermal runaway was detected at the core voltage 2.9 V. During the thermal runaway, the oscillation frequency suddenly starts to fall and correspondingly, power dissipation also falls from 0.36 W at ambient temperature 343 K.

Output drivers are matched for 50-Ohm loads, and these drivers are designed to have two operation modes. Therefore, power consumption of the device shown in Fig. 4 illustrates these operation modes. In low-power mode, the output power varies from -6 dBm to 0 dBm depending on the oscillation frequency. In high-power mode, the output power is constant at 0 dBm regardless of the oscillation frequency thus solving the existing problems of the variable output level of a conventional ring oscillator [1].

Fig. 6 shows the measured phase noise of the proposed oscillator where the up-conversion corner frequency of flicker noise is determined to be 2.3 MHz. In the figure, the measured amplitude noise is also shown where it is below the phase noise floor. This is another advantage of a typical saturated mode oscillator. Both noise curves shown in the figure are measured using a Signal Source Analyzer (E5052 B SSA, Agilent Technologies) and keeping the DUT inside a small shielded chamber. Fig. 5 shows the measured tuning range of the oscillator where tuning sensitivity is measured to be 2.9 MHz/mV in linear range. The tuning curve does not depend on the output driver's mode. Figure of merit (FOM) of the ring oscillator is determined from (1) and compared in Table I with other published quadrature
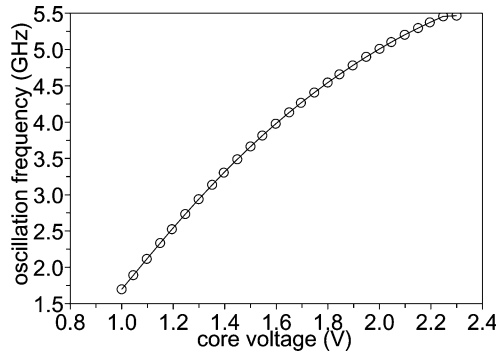
Fig. 5. Measured tuning curve of the quadrature ring oscillator.

Ref.	F_{osc} (GHz)	PN, (dBc)	F_{off} (MHz)	FOM (dB)	Power, (mW)	Tech.
[3]	9.8-11.					0.50μm
	5	-98	2	-153.1	75	
[6]	3.1–6.3	-101.4	1	-155.4	157	0.18μm
[7]	0.1–3.5	-106	4	-152.7	16	0.18μm
[8]	2.5–5.2	-90.1	1	-148.9	17	0.18μm
This work	1.7–5.5	-120.2	4	-162.2	81	0.18μm

tion-assistance transistors in each inverter is proposed and implemented in $0.18 \, \mu m$ CMOS technology. The prototype circuit demonstrates a maximum frequency of 5.5 GHz, and the FOM is −162 dB which is approximately 8 dB improvement than a conventional three-stage ring oscillator.
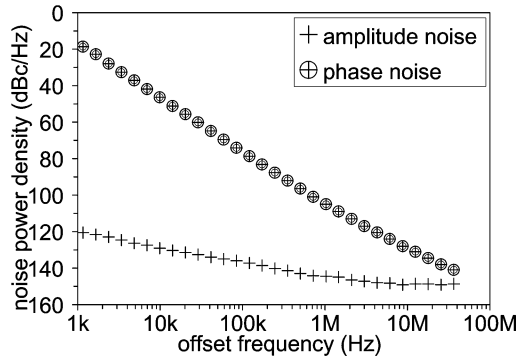

Fig. 6. Measured phase noise and amplitude noise at 4.46 GHz.

ring oscillators where FOM of the proposed oscillator is the best among the designs proposed so far in the same technology

$$FOM = -20\log\left(\frac{F_{osc}}{F_{off}}\right) + PN + 10\log\left(\frac{P_{diss}}{0.001}\right). \quad (1)$$

Where, F_{osc} is the central frequency of oscillation, F_{off} is the offset frequency where phase noise is measured, PN is the phase noise below carrier, and P_{diss} is the dc power consumption.

IV. CONCLUSION

A novel design of a quadrature ring oscillator that employs two-stages differential topology with additional pair of transi-

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