A 3.0-7.5 GHz CMOS UWB PA for Group 1~3 MB-OFDM Application Using Current-Reused and Shunt-Shunt Feedback

S.A.Z Murad, R.K Pokharel, H. Kanaya and K. Yoshida
Graduate School of Information Sciences and Electrical Engineering, Kyushu University
Fukuoka 819-0395 Japan
murad@yossvr3.ed.kyushu-u.ac.jp

S.A.Z Murad
School of Microelectronic Engineering
Universiti Malaysia Perlis (UniMAP)
P.O Box 77, d/a Pejabat Pos Besar, 01000 Kanger, Perlis, Malaysia (On study leave)
sohiful@unimap.edu.my

Abstract— **The design of a 3.0-7.5 GHz UWB CMOS power amplifier (PA) for group 1~3 MB-OFDM UWB applications in TSMC 0.18-µm CMOS technology is presented. The UWB PA proposed in this paper uses a current-reused technique to enhance the gain at the upper end of the desired band, and the resistive feedback at the second stage is used to obtain gain flatness. The shunt-shunt feedback is used to enhance bandwidth and improve output wideband matching. In addition, the cascode topology with an additional common-source stage was used to achieve high power gain. The post-layout simulation results indicated that the input return loss (S11) was less than -5 dB, output return loss (S22) was less than -7 dBm, and average gain was approximately 10 dB over the frequencies ranges of interest. The output 1-dB compression point above 0 dBm, the output third-order intercept point (OIP3) was 10 dBm, and average PAE of 12%. Moreover, an excellent phase linearity property (group delay) of ±137.7 ps across the whole band was obtained with a power consumption of 15 mW.**

Keywords- power amplifier; ultra-wideband; current- reused; cascode; phase linearity

I. INTRODUCTION

Recently, ultra wideband (UWB) technology is actively investigated many researchers in both academic and industrial due to the wide spectrum of frequency bands for very high data rate up to 480Mb/s with very low power over short distances [1]. This wireless technology is becoming more and more popular in many applications and the need to build compact, low cost and low power blocks arises. Therefore, CMOS technology is a good solution due to the advantages of low price, small size, high integration, and low power consumption [2]. Since the FCC allocated the frequency spectrum for UWB technology is 3.1-10.6 GHz, the power level from the UWB transmitter should be small enough not to interfere with the already existing communication systems such as WLAN, Bluetooth and GSM [3]. This mandates the use of low output power levels is limited at -41.25 dBm/MHz.

Until now, several proposals have been presented to realize a short range high data rate wireless applications. One of a standard are under consideration for UWB system is Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) proposed by WiMedia [4]. In this proposal, there are 14 bands within the frequency range from 3.1 GHz to 10.6 GHz is divided into 14 channels with 528 MHz for each channel. All 14 channels are divided into five groups, which each group consists of three channels and the last group consist only two channels. The first three groups from 3.1 GHz to 7.92 GHz are donated as Group 1, Group 2 and Group 3 as shown in figure 1 in [2]. Based on this proposal, the wideband and low power circuits are required especially to RF front end blocks such as PA, low noise amplifier (LNA) and mixer in UWB transceiver and the main challenging to realize the UWB system.

The UWB PAs for the frequency band of 3.0-5.0 GHz (Group 1) and 3.1-10.6 GHz (Group 1 to Group 5) have been widely implemented in the CMOS technology [5]-[8]. Another UWB PA was reported for the frequency band of 6-10 GHz (Group 3 to Group 5) with an inter-stage wideband impedance transformer [9].

In this paper, broadband CMOS power amplifier from 3.0 to 7.5 GHz for group 1~3 MB-OFDM UWB applications is presented. Since the output power level of UWB signals must be too low in order to match the power mask of FCC [1], the proposed design only focused on bandwidth, linearity and power consumption of the UWB PA. The single-ended topology is employed because most existing components designed to be driven by PAs are single-ended. Using cascode topology with additional common source allows increasing power gain. The current- reused technique helps to enhance the gain at the upper end of the desired band and the resistive feedback at the second stage is used to obtain gain flatness. The shunt-shunt feedback is used to increase bandwidth and improve output wideband matching.

II. CIRCUIT IMPLEMENTATION

The proposed design of UWB PA circuit can be divided into two stages as shown in Fig. 1. The first stage consists of

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current-reused cascoded common source (CS) structure, where the M1 and M2 are two CS amplifiers. M2 is also CS amplifier converting from a common gate (CG) amplifier by the current-reused technique. The impedance of L2 is adequately large to provide a high impedance path to block the signal at the desired bandwidth, while the L3 and C3 of M2 provide a low impedance path. Therefore, the input signal can be amplifier twice under this technique. A narrow band characteristic composed by the resonate circuit of L3 and C3 is employed to enhance the gain at the upper end of the desired band. In addition, L5 is inductive peaking to achieve high gain at higher frequency. Capacitor C1 is DC blocking and inductor L1 is part of the input matching, while C2 is the bypass capacitor, and R2 is the bias resistor of M2. M1 transistor is biased in class AB to achieve sufficient linearity and efficiency with the size of 8μm/0.18μm for delivering high output power. M2 transistor is size of 1.5μm/0.18μm draws 1.1 mA current from 1.8 V power supply.

The first stage and second stage are connected with inter-stage inductor L4, and inter-stage capacitor C4, for matching purpose between the first stage and the second stage amplifier and also to enhance the gain. The second stage is CS amplifier with resistive shunt feedback R3 to obtain flat gain and also for biasing M3. M3 with size of 2μm/0.18μm draws 13 mA current from 1.0 V power supply. The shunt-shunt feedback of R4 and C5 is used to enhance the bandwidth and improve wider output matching. It results in lower output impedances. The capacitor C5 is also used to prevent the DC current from flowing directly through the shunt-shunt feedback path to the output terminal. While inductor L6 is a load for CS amplifier of M3 and inductor L7 is used to achieve output matching. The capacitor C6 at the output terminal is DC block.

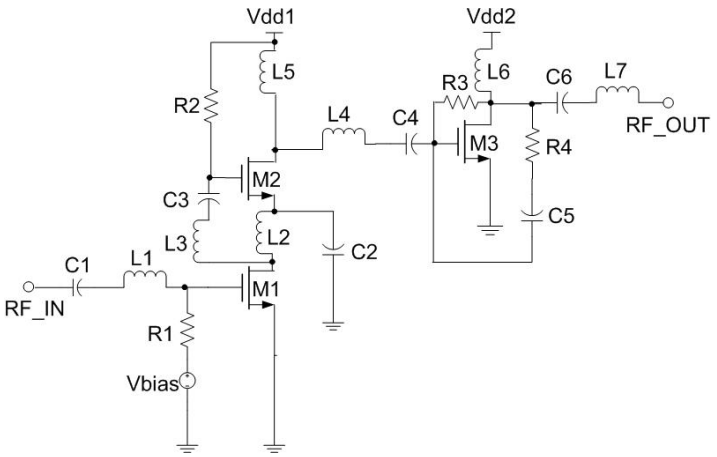

Figure 1. Complete schematic of the proposed 3.0-7.5 GHz CMOS UWB PA.

III. SIMULATION RESULTS

The circuit design of UWB PA is simulated using Cadence SpectraRF simulator in TSMC 0.18-μm CMOS process. Fig. 2 shows the post-layout simulation for small signal gain, input and output return loss using S-parameter analysis. The average gain is obtained about 10 dB from 3.0 GHz to 7.5 GHz. The maximum gain is 13 dB is achieved at 4 GHz. The simulation results also show that the corner frequencies of 3.0 GHz to 8.0 GHz, which are covered for Group 1, Group 2 and Group 3 of MB-OFDM UWB applications. The input return loss, S11 is less than -5 dB and the output return loss, S22 is less than -7 dB is achieved over the frequency ranges of interest. The other S-parameter including insertion loss, S12 is obtained less than -35 dB as shown in Fig. 3 across the whole band.

The gain is a major performance merit for a power amplifier; however, the linearity is also important. The linearity limits the actual power that can be driven to the load by the PA [7]. The PA can drive the wanted signal without too many harmonic terms only in linear region operation. Two typical linearity merits are output 1-dB compression point (P1dB) and third order intercept point IIP3 (OIP3), which represented the nonlinear gain compression and intermodulation effects respectively [7]. The linearity of the PA is simulated using a periodic steady state (PSS). The input 1-dB compression is more than -10 dBm and the output 1-dB compression more than 0 dBm is achieved for the whole band as shown in Fig. 4. In Fig 5, the IIP3 and OIP3 of this UWB PA are about -2.1 dBm and 10 dBm at 5 GHz, respectively.

Phase dispersion is also an important specification for wideband communications [8]. The group delay can be used to indicate the dispersion of transmission phase within signal bandwidth. By definition, group delay is the derivation of the phase of S21 where any resonance in the signal path (or pole in S21) will contribute distortion to the group delay [10]. Thus, as shown in Fig. 6, the group delay variation is only ±137.7 ps within the frequency ranges of interest is obtained by the proposed UWB PA.

Finally, Fig. 7 shows the simulated power added efficiency (PAE) vs. input power (Pin). As it can be seen from the simulation results, the PAE are 8% at 3 GHz, 12% at 5 GHz and 18% at 7 GHz. The average PAE is obtained about 12% for the whole band. The layout of the proposed UWB PA is presented in Fig. 8. The die area including the pads is 0.85 mm × 1.03 mm; this layout is going to tape out for fabrication in the near future.

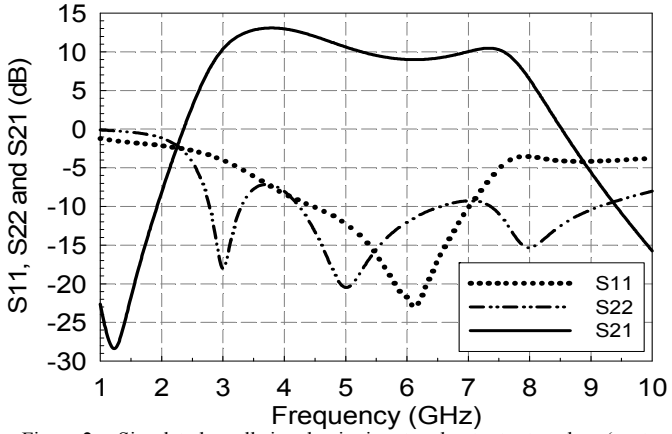

Figure 2. Simulated small signal gain, input and output return loss (post-layout).

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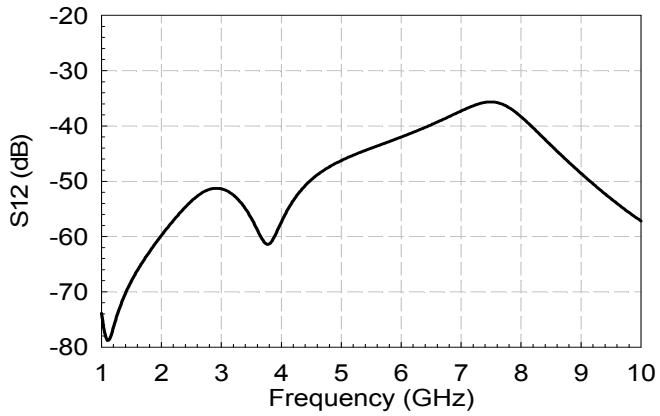

Figure 3. Simulated insertion loss S12 (post-layout).

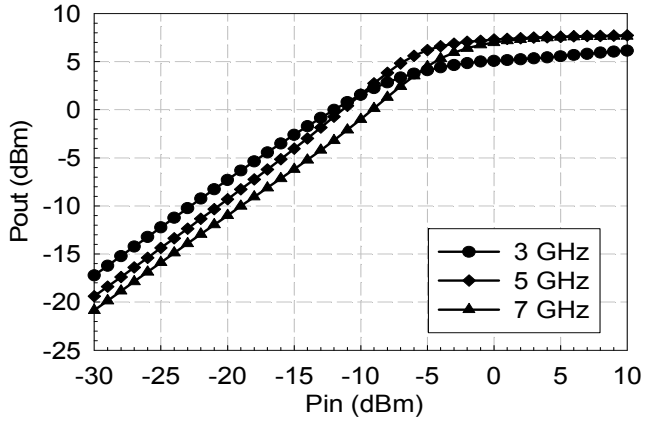

Figure 4. Simulated 1-dB compression point (post-layout).

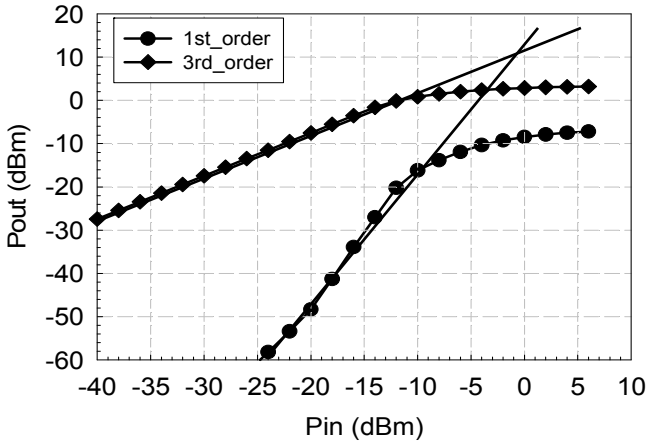

Figure 5. Simulated input and output 3rd order intercept point (IIP3 and OIP3) at 5 GHz (post-layout).

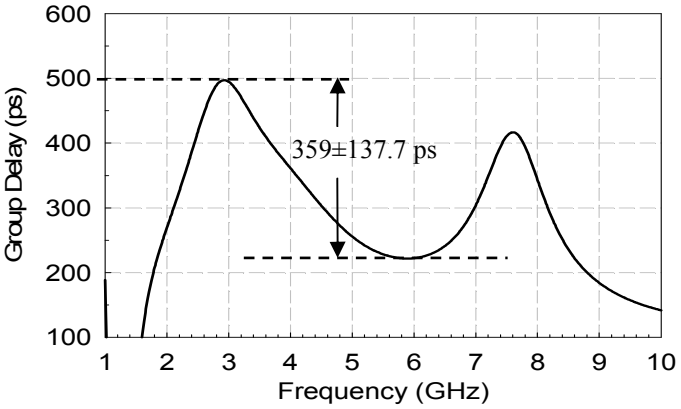

Figure 6. Simulated group delay vs. frequency (post-layout).

Table 1 shows the summary of performances and comparison the previously reported UWB PA and this work. Reference [6] design was implemented two-stage cascaded configuration with shunt-shunt feedback to obtain the higher gain and ultra wide bandwidth for the lower band of UWB frequency, but the PAE was low and consume large chip size. In [7] was proposed full-band UWB PA using wideband RLC matching method, however the PAE was very poor. Reference [8] was designed full-band UWB PA using a combined high-pass and low-pass artificial transmission line architecture had achieved good gain and good input and output matching, but with the large chip size and large group delay variation. Finally, reference [9] was designed a fully integrated 6-10 GHz UWB PA with an inter-stage wideband impedance transformer. The proposed design obtained good PAE and low power consumption. However the gain was quite low.

In contrast, the proposed design in this work obtained good gain, good PAE with lower power consumption and smaller variation of group delay. Moreover, the chip size area also decreased.

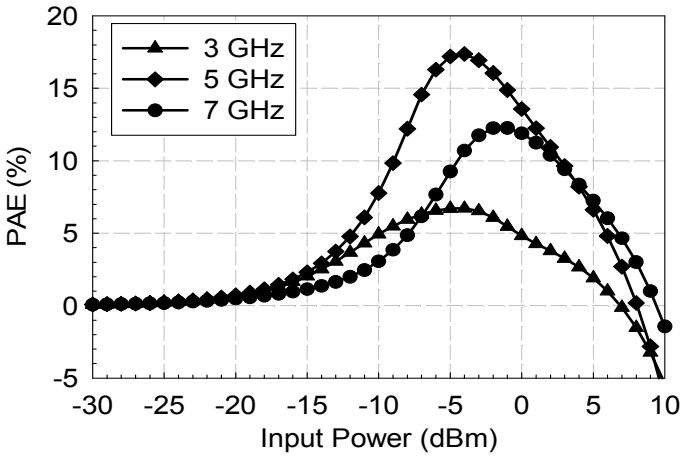

Figure 7. Simulated input power vs. PAE (post-layout).

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IV. CONCLUSION

In this paper, a 3.0-7.5 GHz CMOS PA for UWB applications using current-reused and shunt-shunt feedback is presented. The proposed UWB PA is aiming for Group 1~3 of MB-OFDM UWB transmitter has been implemented in TSMC 0.18-μm CMOS process. The single-ended topology is employed because most antennas designed to be driven by PAs are single-ended. The current-reused technique is clearly helped to increase the gain at the upper end of the desired band while shunt-shunt feedback at the second stage amplifier providing wideband output matching. The cascade with an additional common source stage topology is used to increase high gain and the resistive feedback helps to improve gain flatness. The post-layout simulation shows that the proposed design has reduced power consumption and chip size with good gain and PAE. Moreover, good phase linearity is achieved for the whole frequency ranges of interest.

TABLE I. SUMMARY AND COMPARISON OF UWB PA PERFORMANCES

Reference	[6]	[7]	[8]	[9]	This work
Technology (μm)	0.18	0.18	0.18	0.18	0.18
Supply voltage (V)	3.0-5.0	3.1-10.6	3.0-10.0	6.0-10.0	3.0-7.5
Frequency (GHz)	N/A	1.8	2.0	1.5	1.8
S11(dB)	<-10	<-6	<-10	<-7	<-5
S22 (dB)	<-10	<-8	<-10	<-3	<-7
Average Gain (dB)	19	9	11	8.5	10
OP_{1dB} (dBm)	0.42 (@4 GHz)	>0	8	5	>0
IIP3 (dBm)	N/A	-5	>7.6	N/A	-2.1
OIP3 (dBm)	N/A	6 (@5 GHz)	>16.6	N/A	10 (@5 GHz)
PAE (%)	3.9 (@4 GHz)	3.3	6.8	14.4	12
GD (ps)	N/A	N/A	±250	N/A	±137.7
Power consumption (mW)	N/A	25.2	84	18	15
Chip size (mm^2)	1.52	1.10	1.76	1.08	0.88

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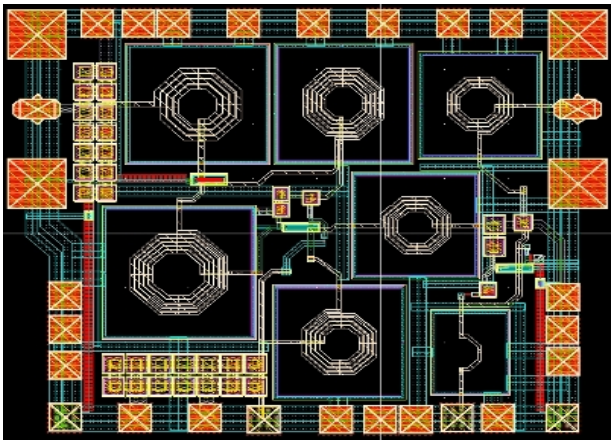

Figure 7. Layout of the proposed 3.0-7.5 GHz CMOS UWB PA on 0.18-μm CMOS technology (0.85mm x 1.03mm).

REFERENCES

[1] FCC (2002), First Report and Order. [Online]. Available: http://www.fcc.gov/Bureaus/Engineering_Technology/Orders/2002/fcc02048.pdf.

[2] W-C. Wang, C-P. Liao, Y-K. Lo, Z-D. Huang, F.R Shahroury, and C-Y. Wu, "The design of integrated 3-GHz to 11-GHz CMOS transmitter for full-band ultra-wideband (UWB) applications," IEEE International Symposium on Journal of Circuits and Systems, 18-21 May, 2008, pp. 2709-2712.

[3] S. Jose, "Design of RF CMOS power amplifier for UWB application," Msc. in Electrical Eng. thesis, Virginia Polytechnic Institute and State University, Virginia, USA, Dec. 2004.

[4] "Multi-band OFDM physical layer proposal for IEEE 802.15 task group 31," IEEE P802.15 Working Group for Wireless Personal Area Networks, Mar. 2004.

[5] S.Jose, H.J Lee & D. Ha, "A low power CMOS PA for UWB applications," IEEE Int. Symposium on Circuits & Systems, ISCAS 2005, vol. 5, pp. 5111-5114.

[6] Ruey-Lue Wang, Yan-Kuin Su, Chien-Hsuan Liu, "3~5 GHz cascoded UWB power amplifier," IEEE Asia Pacific Conference on Circuits and Systems 2006, 4-7 Dec. 2006, pp. 367 – 369.

[7] Han Chou Hsu, Zhi Wei Wang & Gin Kou Ma, "A low power CMOS full-band UWB power amplifier using wideband RLC matching method," IEEE Conference on Electron Devices and Solid-State Circuits , pp. 233-236, 19-21 Dec. 2005.

[8] C. Lu, A-V. Pham, and M. Shaw, "A CMOS power amplifier for full-band UWB transmitters," IEEE Radio Frequency Integrated Circuits (RFIC) Symposium 2006, 11-13 June 2006, p. 400.

[9] H.-W Chung, Hsu, C.-Y.; Yang, C.-Y; Wei, K.-F.; Chuang, H.-R., "A 6-10-GHz CMOS Power Amplifier with an Inter-stage Wideband Impedance Transformer for UWB Transmitters," 38th European Microwave Conference, 27-31 Oct. 2008, pp. 305-308.

[10] C-Z. Chen, J-H. Lee, C-C. Chen and Y-S. Lin, "An Excellent Phase-Linearity 3.1-10.6 GHz CMOS UWB LNA Using Standard 0.18 μm CMOS technology," Proceedings of Asia-Pasific Microwave Conference, 2007.