A Low Flicker Noise Direct Conversion Receiver for the IEEE 802.11a Wireless LAN Standard

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***Abstract* — In this paper, a low flicker noise, 5 GHz Direct Conversion Receiver (DRC) has been designed utilizing Dynamic Current Injection (DCI) and tuning inductor in the mixing stage. This DRC has been designed in a TSMC 0.18 µm 1P6M CMOS process for WLAN 802.11a applications. The proposed DRC achieves 7.4 dB SSB-NF, 28 dB Conversion Gain (CG), -10 dBm IIP3, and *1/f* noise corner frequency of 100KHz with 80mW power consumption from 1.8V supply voltage. The active chip area was 1.9mm^2. All the simulations has been performed by Cadence Spectre® simulator.**

***Index Terms* — Front-End receiver, IEEE 802.11a, CMOS analog integrated circuits, Direct conversion receiver, flicker-noise.**

I. Introduction

In the past several years, the demand for wireless LAN (WLAN) technology has grown significantly. Along with this growth in demand has come an increased interest in more than the maximum 11 Mb/s offered by the 802.11b standard. The IEEE 802.11a WLAN protocol provides data rates up to 54 Mb/s using a 20-MHz channel bandwidth in the 5-GHz unlicensed national information infrastructure (UNII) band. The data is modulated with BPSK, QPSK, 16QAM, or 64QAM, and further mapped into 52 subcarriers of an orthogonal frequency division multiplexing (OFDM) signal [1]. In order to realize WLAN 802.11a standard with CMOS analog integrated circuits, suitable receiver architecture should be selected. Direct conversion architecture is one of the best candidates to realize highly integrated solutions for wireless applications. Direct conversion, also called zero-IF, is the natural approach to downconverting a signal from RF to baseband. It translates the band of interest directly to zero frequency and employs low-pass filtering to suppress nearby interferers. Among this the DRC have a few drawbacks: flicker noise, dc offset, even-order distortion, and LO leakage [2]. Flicker noise is a critical issue in DRC design as it almost degrades the signal-to-noise ratio (SNR) and total noise figure, which results in the degradation of receiver sensitivity. Most of the flicker noise contribution comes from the mixer stage, which should be design carefully to reduce the output flicker noise. A dynamic current injection technique with a tuning inductor has been employed in the mixer design in order to reduce the output 1/f noise corner frequency.

II. Receiver Architecture

The basic block-diagram for DRC receivers is illustrated in Fig. 1. The receiver comprises a Low Noise Amplifier (LNA) followed by active balun used to convert single ended LNA output to a differential signal suitable to feed the double balanced Gilbert cell mixer.

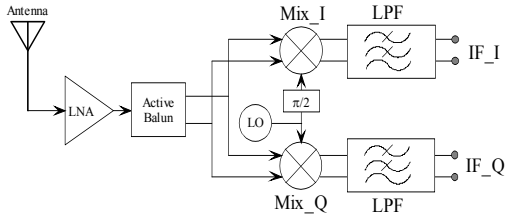

Fig. 1. Block diagram of direct conversion receiver system.

Since the quadrature I and Q channels are necessary in typical phase- and frequency-modulated signals because the two sidebands of the RF spectrum contain different information and result in irreversible corruption if they overlap each other without being separated into two phases [2], two mixers have been used to downconvert the RF signal to a quadrature BB signal. The mixer is followed by an on-chip low-pass filter to produce the necessary filtering and decrease LO and RF leakage to the output Base-Band (BB) signal. LO signal supplied to the receiver externally, but the quadrature LO signal generated on chip using a poly phase filter. A full detailed description of each block as following:

A. LNA

A resistive feedback and an inductive peaking technique is employed to achieve higher gain in the band of WLAN at 5GHz. Negative feedback resistor also improves the stability factor (K) to provide unconditional stability of the amplifier and reduce the gain sensitivity [3] [4]. Fig. 2 shows a LNA circuit.

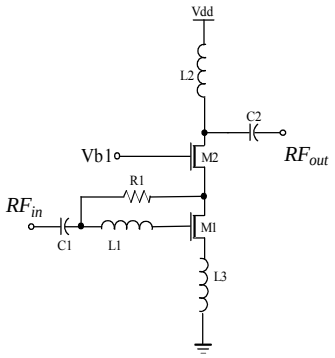

Fig. 2. LNA circuit.

A cascade amplifier consists of M1 and M2 with R1 resistive shunt feedback used to supply feedback current to the

input, by proper selection of R1 value, it can helps significantly to achieve input matching with C1 and L1. Degenerative inductor L3 used for simultaneous input and noise matching.

B. Active Balun

Single-ended input LNAs are commonly used because antennas and RF filters usually produce single ended signals. On the other hand, differential signaling in the receive chain is preferred in order to reduce second order distortion and to reject power supply and substrate noise. Thus, at some point in the receive chain a balun is needed to convert the single-ended RF signal into a differential signal [5]. Fig. 3 shows the circuit diagram for the active balun. The input signal is amplified via two paths, a non-inverting Common Gate (CG) path, M3 and R3 with L4 as load, and an inverting Common Source (CS) path, M4 with inductive load L5. The voltage gains of these two paths are designed to be equal, giving the balun function.

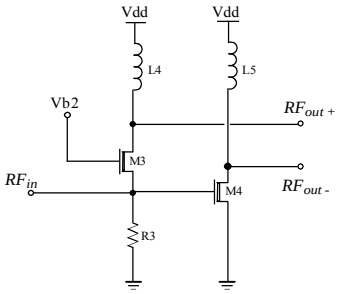

Fig. 3. Active balun circuit.

The phase difference of the active balun can be calculated as follow [6]:

$$(\angle S_{21})_{CS} - (\angle S_{21})_{CG} = \tan^{-1}\left(\frac{-g_m \omega C_{gs} Z_0^2}{1 + g_m Z_0 + \omega^2 C_{gs}^2 Z_0^2}\right) \quad (1)$$

where Z_0 is the characteristic impedance termination (50Ω). By proper sizing and biasing of M3 and M4, the phase mismatch can be minimized for the band of interest. This balun has broad band performance and low power consumption. Fig. 4 shows the phase and amplitude mismatch over the full band. It is clear that the active balun circuit exhibits less than 0.4dB of amplitude mismatch and less than 2^o degree of phase mismatch around the 5 GHz band.

C. Poly-phase filter

A poly-phase filter can be used for generation of the four-phase orthogonal LO signals with phases of $0^o/90^o/180^o/270^o$ around 5GHz pole. A poly-phase filter is a symmetric RC network that decomposes its inputs and outputs into different phases symmetrically. A simple differential-to-quadrature poly-phase filter is shown in Fig. 5. The passing frequency is defined by a single RC pole as [7]:

$$f_0 = 1/(2\pi RC) \quad (2)$$

A differential LO signal connected to the chip using five contacts *Air Coplanar Probe* (GSGSG) with 100μm pitch for measurement purpose.

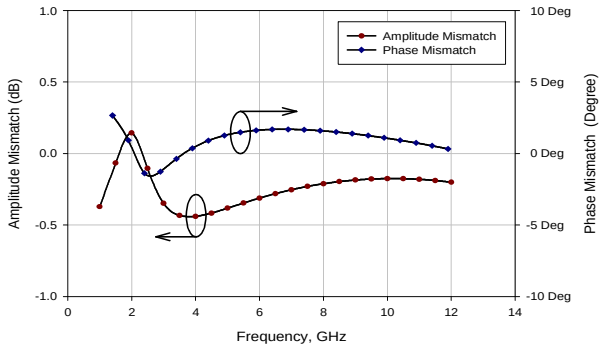

Fig. 4. Amplitude and phase mismatch of the active balun circuit.

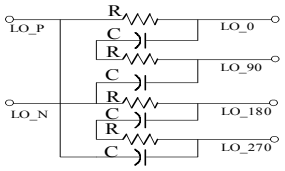

Fig. 5. A single pole poly-phase filter.

D. Double Balanced Gilbert Cell Mixer

A commonly used active mixer in CMOS system is the Gilbert mixer. Double balanced is just a combination of two single balanced Gilbert cell connected in parallel as shown in Fig. 6. This comprises an input differential transconductance stage formed by M5 and M6, a pair of mixer switching cores formed by M9-M12 and an output load, *ploy resistor which is free of flicker noise load* has been used in this design. Highly linear mixer design with low flicker noise output will be shown in details in next section.

III. Highly Linear Low Flicker Noise Double Balanced Gilbert Cell Mixer

In the proposed mixer design, two important issues have been considered significantly, one is the flicker noise at the mixer output; the other is the mixer linearity.

A. Flicker Noise Mechanisms in Gilbert Cell Mixers

Flicker noise has a great effect in mixer circuits while the other RF circuits don't affected by the flicker noise, such as low noise amplifiers (LNA), since its operating frequency is much higher than the flicker noise corner frequency [8], but in the mixers, the case is different, because the flicker noise lies in the output band of the mixer, specially, Zero-IF receivers.

Mainly there are two major mechanisms that generate the flicker noise of the switching pair devices M9-M12. The first one is the *direct mechanism*, due to the finite slope of the switching pair transitions. In order to decrease flicker noise in the direct mechanism, the size of the switching pairs needs to be increased, and large switching devices increase the parasitic capacitance of the switching pairs, resulting in the flicker noise indirectly translating to the output. The second mechanism that generates flicker-noise is the *indirect mechanism*, flicker-noise mainly depends on the tail capacitance (*Cp*) at the node between the LO switches and RF transconductance stage [9]. In order to decrease the flicker noise in CMOS active mixers, the bias current of the local oscillator (LO) switches should be small enough to lower the height of the noise pulses.

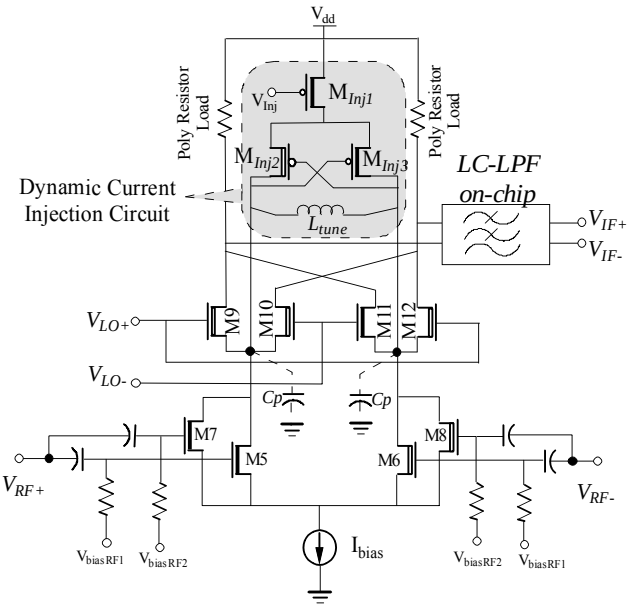

Fig. 6. Proposed Gilbert cell mixer with DCI and DS techniques.

The static current injection technique was proposed to reduce the bias current of the LO switches [10]. However, the impedance of the LO switches seen from the RF stage is increased as we reduce the bias current of the LO switches. In addition, RF leakage current flows through the injection circuit, which decreases conversion gain and also allows more RF current to be shunted by the tail capacitance (*Cp*) at the node between the LO switches and RF transconductance stage. Dynamic Current Injection (DCI) proposed in [11] [12]. DCI technique has been used in the proposed mixer in order to reduce *direct* flicker-noise generation. As shown in Fig.6, three pMOS, M_{inj1} through M_{inj3}, used to inject a dynamic current equal to the bias current of each pair of switches at only the switching event. *Vinj* is used to control the height of the injected current pulses. A parallel tuning inductor L_{tune} has been employed to tune out the parasitic tail capacitances (*Cp*) to alleviate the indirect flicker noise source. Fig. 7 shows the mixer noise figure with and without DCI, it's clear how the flicker noise corner frequency reduced significantly.

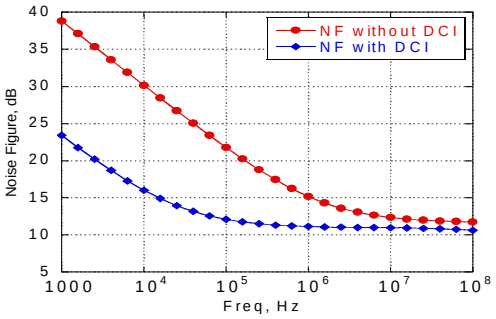

Fig. 7. Noise figure comparison between conventional mixer and proposed one.

B. Mixer Linearity improvements using Derivative Superposition (DS) Technique.

The linearity of mixer in a receiver is one of key issues because the whole linearity of a receiver is often limited by the down-conversion mixer due to a relatively large signal level compared with the input signal level of LNA. Intermodulation distortion in the mixer greatly affects the dynamic range of most communication systems. Therefore, the mixer determines the achievable second-order input intercept point (IIP2) and third-order input intercept point (IIP3) of the receiver. In CMOS downconversion mixers, there are several mechanisms which generate intermodulation distortion [13]: self-mixing, transconductor nonlinearity, switching pairs nonlinearity, and mismatch in load resistors. Due to coupling into the local oscillator port, the RF signals self-mix. Self-mixing can be significantly reduced by means of layout techniques which decrease coupling effects between the RF and LO signals. Active devices inherently generate second-order intermodulation distortion components because they have nonlinearities in the I-V characteristic. Several linearization methods have been proposed for high linear CMOS mixers, one of the successful linearization techniques is the derivative superposition (DS) technique [12]. This method cancels the negative third order nonlinearity of the MOSFET's dc transfer characteristic g_3, where g_3 is the third order variation of the drain current with V_{gs} voltage($\partial^3 i_d / \partial V_{gs}{}^3$), by paralleling the auxiliary MOSFETs, M7 and M8, biased near the weak inversion region with the positive g_3, as shown in Fig. 8. The mixer circuit followed by an on-chip LPF to filter-out the adjacent channels interferer and reduce the LO and RF leakage to the BB signal.

IV. Simulation Results

Fig. 9 shows the layout of the proposed direct conversion receiver. The chip has been design using TSMC 0.18µm 1P6M CMOS technology. The total chip die area including pads is 1.9mm^2. All the simulations had been done using Cadence Spectre® simulator.

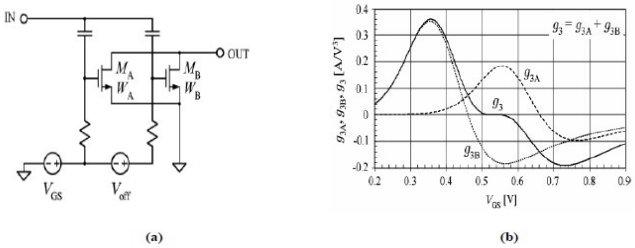

Fig. 8. (a) Schematic of MOSFET linearization using DS technique. (b) Third order power series coefficient.

The core circuit draws 44.7mA from 1.8V supply voltage. Fig. 10 shows the simulated power gain over the band in WLAN, the DRC achieves 28dB maximum conversion gain. The input return loss of RF port is less than -17dB @ 5GHz as shown in Fig. 11. The proposed receiver achieves high IIP3 compared to the low power consumption, the IIP3 of the receiver equal to -10dBm @ LO power of -5 dBm, IIP3 curve shown in Fig. 12. Table 1 shows the summary of the proposed receiver performance.

VI. Conclusion

A low flicker noise highly linear direct conversion receiver for WLAN 11.802a has been proposed and simulated using TSMC 0.18µm technology. The receiver shows a high third order intercept point of -10dBm with 80mW power

consumption and 100KHz flicker noise corner frequency by using a dynamic current injection and drivative superposition techneques. The receiver achieves a 28dB conversion gain and 7.4dB SSB-NF at -5dBm LO power. The receiver consumes 80mW power with 1.8V supply.

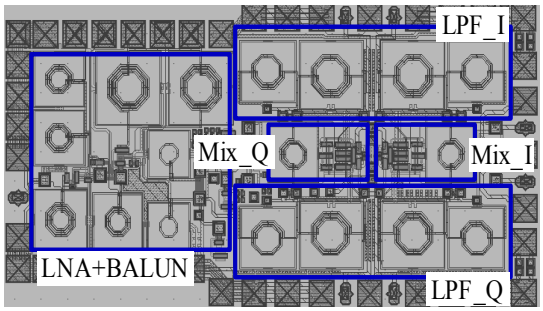

Fig. 9. Layout of the proposed DRC for WLAN.

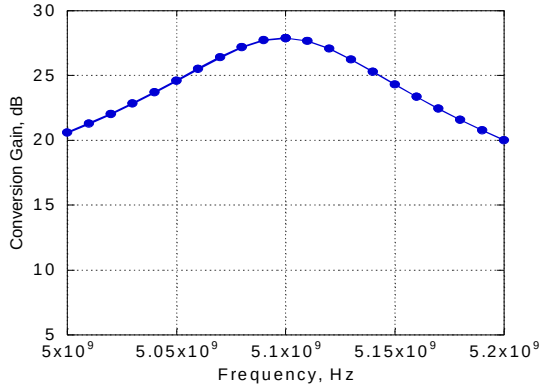

Fig. 10. Conversion gain versus RF frequency.

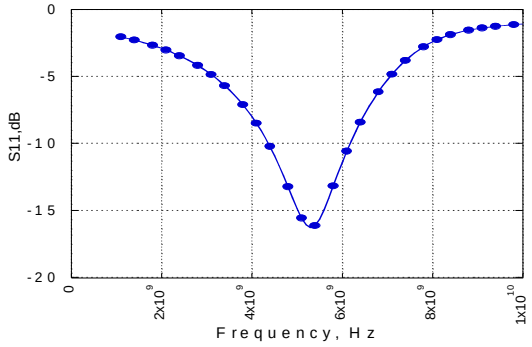

Fig. 11. Input RF return loss (S11) for the proposed receiver.

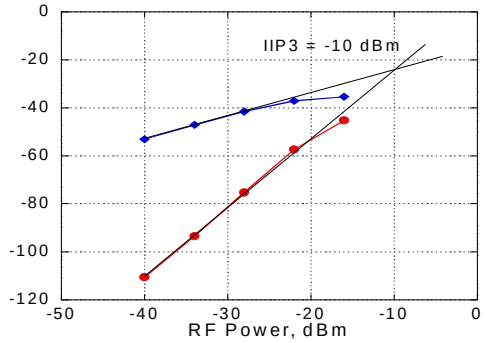

Fig. 12. Third order intercept point (IIP3) of the proposed receiver.

ACKNOWLEDGEMENT

This work was partly supported by a Grant-in-Aid for Scientific Research from JSPS (KAKENHI) and Fukuoka project in the Cooperative Link of Unique Science and Technology for Economy Revitalization (CLUSTER) from Ministry of Education, Culture, Sports, Science and Technology (MEXT). This work was also partly supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with CADENCE Corporation and Agilent.

TABLE I
SUMMARY OF RECEIVER PERFORMANCE

Input Freq.	5 GHz WLAN 802.11a
Noise Figure (SSB)	7.4 dB
IIP3	-10 dBm
Conversion Gain	28 dB
LO Power Input Power	-5 dBm
Return Loss	< -17 dB
1/f Corner Frequency	100KHz
Power Dissipation	80 mW
Technology	TSMC 0.18µm 1P6M
Die Area	1.9 mm^2

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