10 Bit 2/5GHz Dual Band Digitally-Controlled LC-Oscillator in 0.18 um CMOS Process

Ramesh K. Pokharel [#1], Kenta Uchida [*1], Abishek Tomar[#1], Haruichi Kanaya [#1], Keiji Yoshida [#1]

[#]*Graduate School of ISEE, Kyushu University*
Fukuoka 319-0395 Japan
[1]pokharel@ed.kyushu-u.ac.jp
[3]uchida@yossvr3.ed.kyushu-u.ac.jp

***Abstract* — This paper presents a design methodology and verification of a 2/5 GHz dual band digitally-controlled oscillator (DCO). The DCO employed two spiral inductors and a switching transistor controlled by a digital signal is connected between them to operate at two bands, respectively shifting from a frequency to another. The proposed circuit is implemented in 0.18 um CMOS technology and tested. The measured phase noise was –120.5 dBc/Hz and -113.9 dBc/Hz (both @ 1 MHz offset) at carrier frequency of 2.7 GHz and 4.1 GHz, respectively.**

***Index Terms* — Digitally-controlled oscillator, dual band oscillator, phase noise, frequency tuning step.**

I. Introduction

The explosive growth of wireless mobile systems in GHz range has forced the implementation of radio frequency integrated circuit low cost CMOS technology. Scaling down of CMOS technology and reduction in supply voltage complicates the implementation of RF circuits in deep submicron CMOS technology and favors the use of digital-assisted approaches in RF circuit implementation [1]-[3]. A dual band oscillator, being a critical component of all digital phase locked loop (ADPLL) for future generation multi-standard wireless transceiver, is therefore necessary to implement and integrated with the complete system with digitally assisted approaches.

On the other hand, demands for radios which can support multiple bands and multiple standards with minimal hardware implementations attracts a lot of interest in wireless communication systems. An example of such systems is 2.4 GHz/5.2GHz dual-band Wireless Local Area Network (WLAN). The compatibility and high data rate requirement have lead to the desire of integrating 2.4 GHz and 5.2 GHz wireless applications together in a dual band transceiver system. Therefore, an oscillator with a wide tuning range or a oscillator operating at both bands is demanded.

A few of the major issues to mention in a dual-band digitally-controlled oscillator (DCO) design is to shift one frequency band to another and realization of low phase noise in the oscillator core. One of the most popular approaches to switch the operation from one frequency to another is to use a CMOS switch to change either capacitance or inductance. However, the resistance of the CMOS switches is likely to cause the degradation of the tank quality factor (Q) and, consequently, the oscillator's phase-noise. A wide tuning range VCO can be another choice to cover two bands [6], but usually requires a MEMS switch to realize a variable inductance. The DCO implemented in ring structure [3] gives wide turning range but encounters by a poor phase noise performance with high power consumption, and a ring oscillator is, therefore, hardly suitable for multi-GHz wireless communication applications. A set of multiple LC-DCOs can support multiple bands, however, this could be unaffordable in portable devices due to the overwhelming circuit overheads.

In this paper, a switching transistor concept is employed between two inductors for dual operation of the oscillator and the switching operation is controlled by a digital signal. Furthermore, operation of the capacitor banks is fully controlled by 10 bits digital signals so that the oscillator becomes fully digitally controlled. Finally, the proposed DCO is implemented and fabricated in 0.18 um CMOS technology and the concept is verified by testing the chip.

II. Circuit Topology of Dual-Band DCO

The proposed schematic of the dual-band DCO is shown in Figure 1 where the core of the DCO is similar to cross-coupled LC-oscillator [7] [8]. The proposed DCO is consists of three sections-switched inductors, capacitor banks and cross-coupled pmos. This topology is originally similar to a well-known cross-coupled voltage-controlled LC-oscillator except the varacters where capacitance is varied by controlling the supply voltage to the varacters, whereas in our proposed design, the wide-tuning range is realized by controlling the capacitance of capacitor banks digitally. Here, we used 10 bits to control the capacitance of the capacitor bank which, in turn, realize the variable frequency over the tuning range.

The parasitic capacitance of the interconnects affect the frequency of oscillation and the output of the oscillator is connected to the buffer circuits. Two inductors are used in the present study to make DCO to function at two bands. Figure 2 shows the circuit configuration of two inductors connected to each other through the switches. For example, if

Vind is turned off, only L2 becomes effective to generate the oscillating frequency and when Vind is turned on, the effecting inductance of L1 and L2 play the role in LC-tank circuit and in turn, in generating the oscillating frequency.

Figure 3 shows the schematic of capacitor bank which is composed of 20 stacks of the MIM capacitors and MOS switches. The control of the capacitor banks are performed by 10 bits digital signals. When Ck is assumed to be the capacitance of k^{th} bit signal, the oscillation frequency is determined by the following equation, where f is the frequency of oscillation of the inductance (L) and the discrete addition of the capacitance of the capacitance of k^{th} bit and the parasitic capacitance of interconnects. The value of L is chosen by the other set of switches between $L2$ and the parallel combination of $L1$ and $L2$.As the value of inductance changes by switching the switched inductors, the frequency of oscillation can greatly be varied at the wider range.

$$f = \frac{1}{2\pi\sqrt{L(\sum_{k=1}^{10} C_k + C_{para})}}$$

$$(L = L_2 \; or \; \frac{L_1 * L_2}{L_1 + L_2})$$

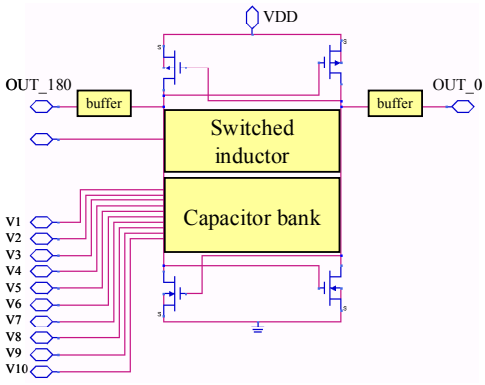


Fig. 1. Circuit topology of the proposed 10 bits DCO.

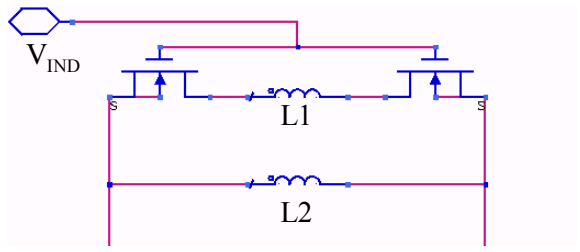


Fig. 2. Circuit configuration of switched inductor parts.

III. Simulation Results

Figure 4 shows the simulated tuning range at two frequency bands controlled by the digital codes. Here, we use 10b digital signals to control the capacitor bank so that the number of digital codes will equal to 1024 (2^{10}). In the higher band, the simulated frequency of oscillation varies from 2.58 GHz to 2.94 GHz where in the higher band, the frequency varies from 4.53 GHz to 5.53 GHz, respectively. Each band is controlled by 10 bit digital signals so that the minimum frequency steps are 780 kHz and 540 kHz at the higher and lower band, respectively. These simulation results shows that the frequency bands covers the dual band operation of WLAN at 2/5 GHz-band operations, respectively.

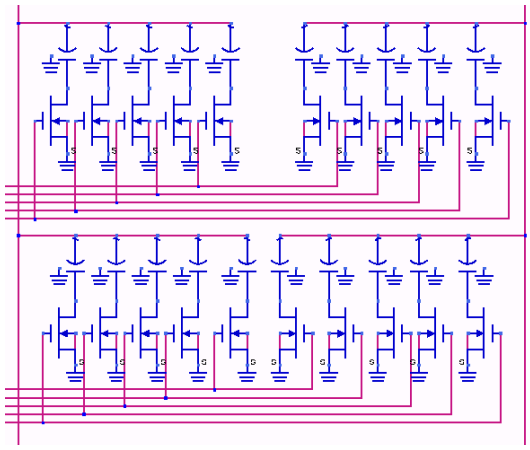


Fig. 3. Circuit topology of capacitor bank.

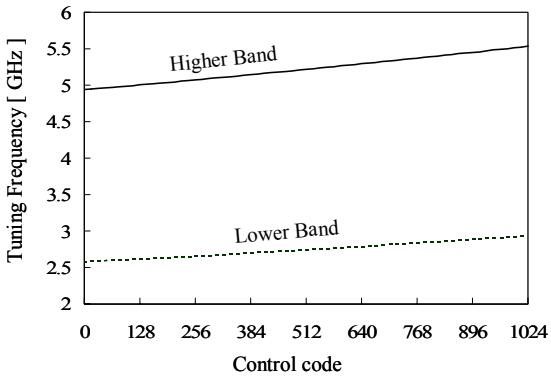


Fig. 4. Frequency tuning ranges of 10 bit dual-band DCO at the two separate frequency bands.

IV. Fabrication and Measurement Results

The control pins were wire bonded to a package and the package was placed on a PCB and externally controlled manually. All pads including digital control inputs, groundings and RF output pads are connected by wire bonds.

The inductance of all wire bonds had been taken into account in the design.

Figure 5 shows the chip photograph of the proposed DCO to test the proposed concept of designing the dual-band operation of a DCO. The output of DCO is designed with buffer circuits to provide a good matching to the measurement equipments. The measured DC power consumed by the DUT was about 74 mW at 1.8 V supply, and simulation shows that about 61% of total power was consumed by the buffer circuits only. The exact power consumption of the proposed DCO can be predicted when two separate DC supply source were designed for DCO core and buffer circuits, respectively.

Phase noise of the DCO was measured using a Signal Source Analyzer (E5052B SSA, Agilent Technologies) and keeping the DUT inside a shield box to protect from the external EM noise to the phase noise measurement. Therefore, the output RF pads of the DUT were wire bonded to PCB as shown in Figure 5 and then to SMA connectors to facilitate to measure the phase noise inside the shield box. The digital controls bits are inputted through the digital pads.

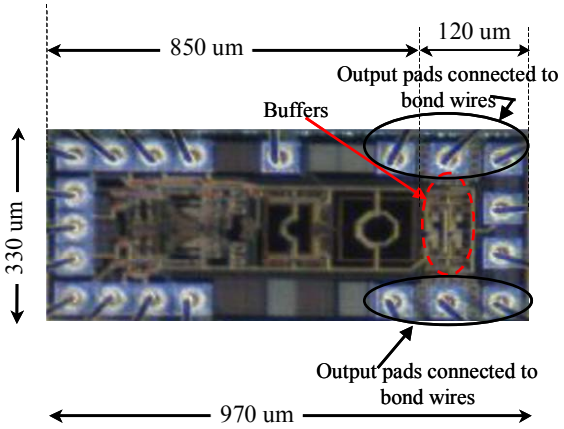


Fig. 5. Chip photograph of 10b dual-band DCO fabricated in 0.18 um CMOS technology.

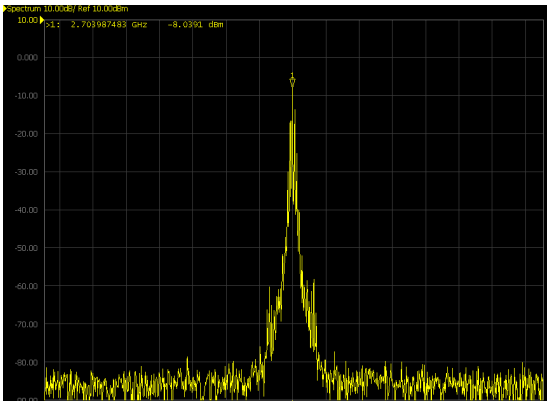
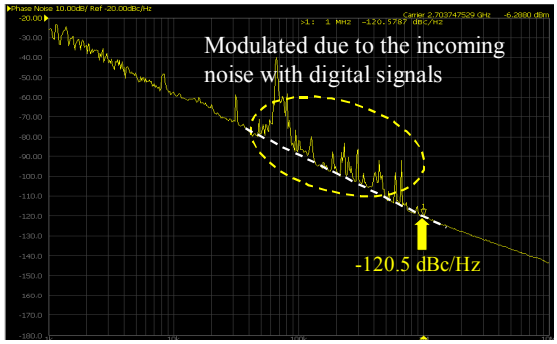
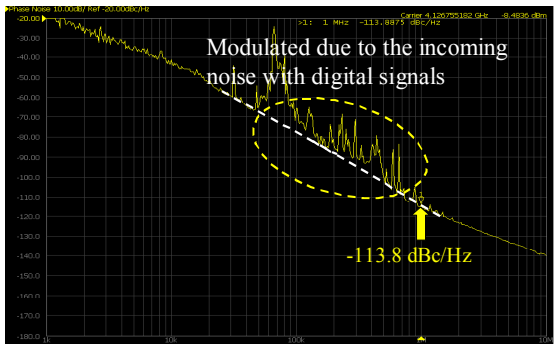


Fig. 6. One of the output spectrums of the 10b DCO at lower band.



(a) Measured phase noise at lower band (Carrier frequency is equal to 2.7 GHz)



(b) Measured phase noise at higher band (Carried frequency is equal to 4.1 GHz)

Fig. 7. Measured phase noise of the dual-band DCO.

Table I shows the comparison of the performance of the proposed DCO and other dual-band VCOs. We took the example of dual-band VCO to compare the results of the proposed dual-band DCO because there was not any dual-band DCOs reported so far to the author's knowledge. In the table, the advantages of the proposed DCO are the smaller size, fine frequency-tuning step, and better phase noise compared. One of the reasons of smaller chip size of the presented DCO is the size reduction due to the non-use of the varacters capacitances. However, the difference in the design results and measured results of the proposed DCO has been observed, especially in the tuning range. This is mainly due to the parasitic capacitance associated with the interconnects and MIM capacitors.

TABLE I. COMPARISION OF THE PROPOSED 10 BIT DUAL BAND DCO WITH RECENTLY REPORTED DUAL-BAND VCOS.

	This DCO	Ref [3]	Ref [4]
Technology	0.18 um CMOS	0.18 um CMOS	0.18um CMOS
Oscillator type	DCO	VCO	VCO
Frequency band [GHz]	2.7/4.11	2.74/5.49	2.62/5.22
Phase noise [dBc/Hz]	-120/-114 (@1MHz)	-135/-126 (@1MHz)	-98/-91 (@100kHz)
Minimum frequency tuning step [kHz]	330/58	NA	NA
Chip size [mm^2]	0.32	0.40	0.71

VI. CONCLUSION

We designed and tested a 10b dual-band DCO for 2/5 GHz wireless applications in 0.18 um CMOS technology. A switched inductor concept was used to realize the dual-band operation of the oscillator, and 10 bits digital signals are used to control the capacitor banks made of MIM capacitors. The DCO has very fine frequency tuning steps of 58 kHz at higher band and 330 kHz at lower band. The other advantages of the proposed DCO are smaller chip size and lower phase noise. The proposed DCO does not consist of varacters which substantially helped to reduce the chip size.

ACKNOWLEDGEMENT

This work was partly supported by a grant of Knowledge Cluster Initiative implemented by Ministry of Education, Culture, Sports, Science and Technology (MEXT), JSPS.KAKENHI (Wakate-B and Kiban-B), and JST-Seeds Excavation (B). This work was also partly supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with CADENCE Corporation and Agilent Technologies.

REFERENCES

[1] R. B. Staszewski, C. Hung, N. Barton, M Lee and D. Leipold, "A digitally controlled oscillator in a 90 nm Digital CMOS process for mobile phones", *IEEE J. Solid-State Circuits*, vol. 40, pp 2203-2211, Nov. 2005.

[2] A. Matsuzawa, "Digital-centric RF CMOS technologies", *IEICE Trans. Electron.*, vol. E91-C, no. 11, pp. 1720-1725, Nov. 2008.

[3] B. Fahs, W. Y. Ali-Ahmad, and P. Gamand, "A two-stage ring oscillator in 0.13-um CMOS for UWB impulse radio," *IEEE Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1074-1082, May 2009.

[4] Lin Jia, Jian Guo Ma, "A 1.8-V 2.4/5.15-GHz Dual-Band LC VCO in 0.18_um CMOS Technology" *IEEE. Microwave and Wireless Components Letters*, vol. 16, pp.194-196, 2006.

[5] Chien-Chih Ho, Chin-Wei Kuo, Chao-Chih Hsiao, Yi-Jen Chan , "A fully integrated dual-band VCO by 0.18 um CMOS technologies" *Solid-State Electronics,* vol. 47 , pp. 2015-2018 , 2003.

[6] Yusaku Ito, Yoshiaki Yoshihara, Hirotaka Sugawara, Kenichi Okada, and Kazuya Masu, "A 1.3-2.8 GHz Wide Range CMOS LC-VCO Using Variable Inductor," *IEEE Asian Solid-State Circuits Conference*, pp.265-268, Nov. 2005

[7] L. Dai and R. Harjani, "Design of high-performance CMOS voltage controlled oscillators," *Kluwer Academic Publishers*, 2003.

[8] A. Hajimiri and T. H. Lee, "The design of low noise oscillators," *Kluwer Academic Publishers*, 2004.