Egypt-Japan University of Science and Technology (E-JUST)

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Contents

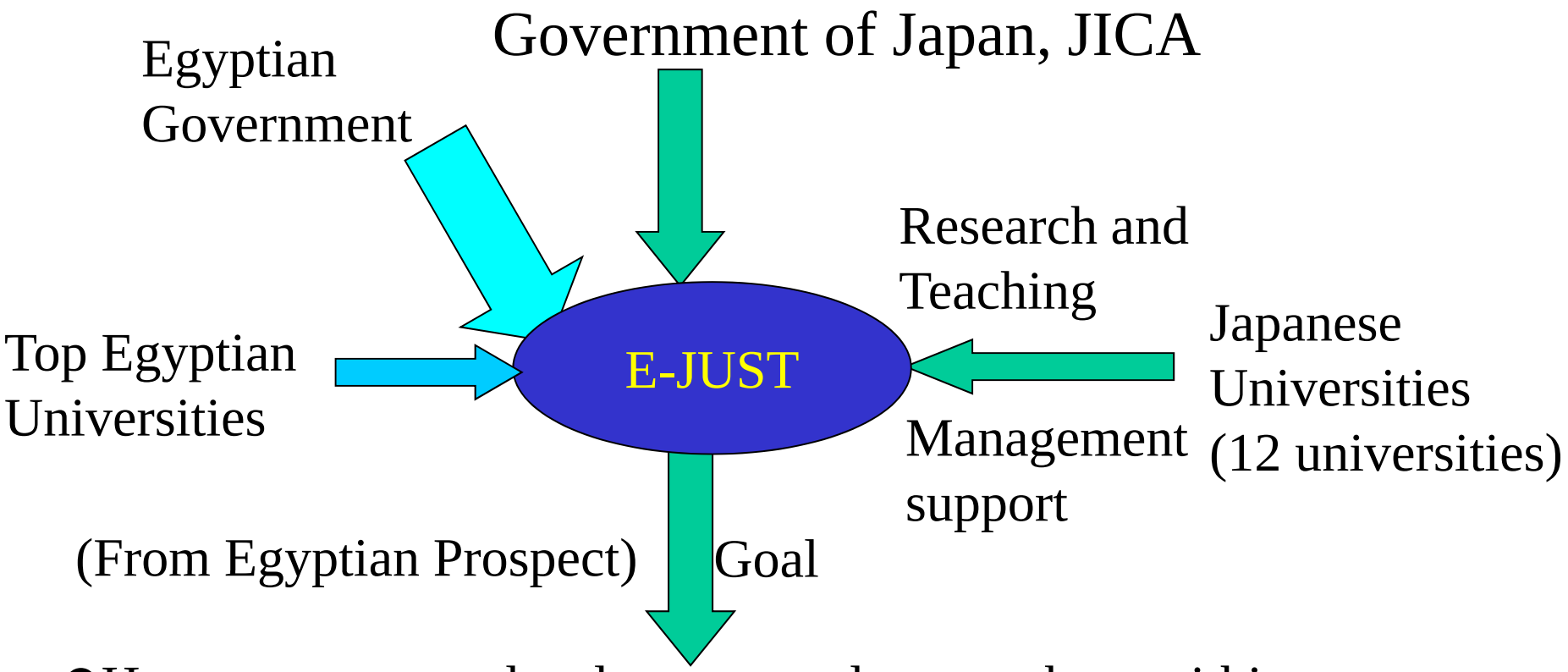
- What is E-JUST?
- How E-JUST functions?
  Two-tier model in research supervision
- How is Kyushu University supporting to E-JUST?
  (As an administrative body for E-JUST's Japanese partners)
- Conclusion

E-JUST: Egypt-Japan University of Science and Technology

- A national project of the Japanese government under JICA's initiative to establish a Japanese-style university in Alexandria, Egypt in corporation to Egyptian government.

- The university is targeting 'world class' research and teaching quality with regional and global reach.

Mechanism of E-JUST



- Human resources development and to trap them within the country.
- Reform of Science and Tech.Higher education in Egypt.
- Top 500 University in 10 years

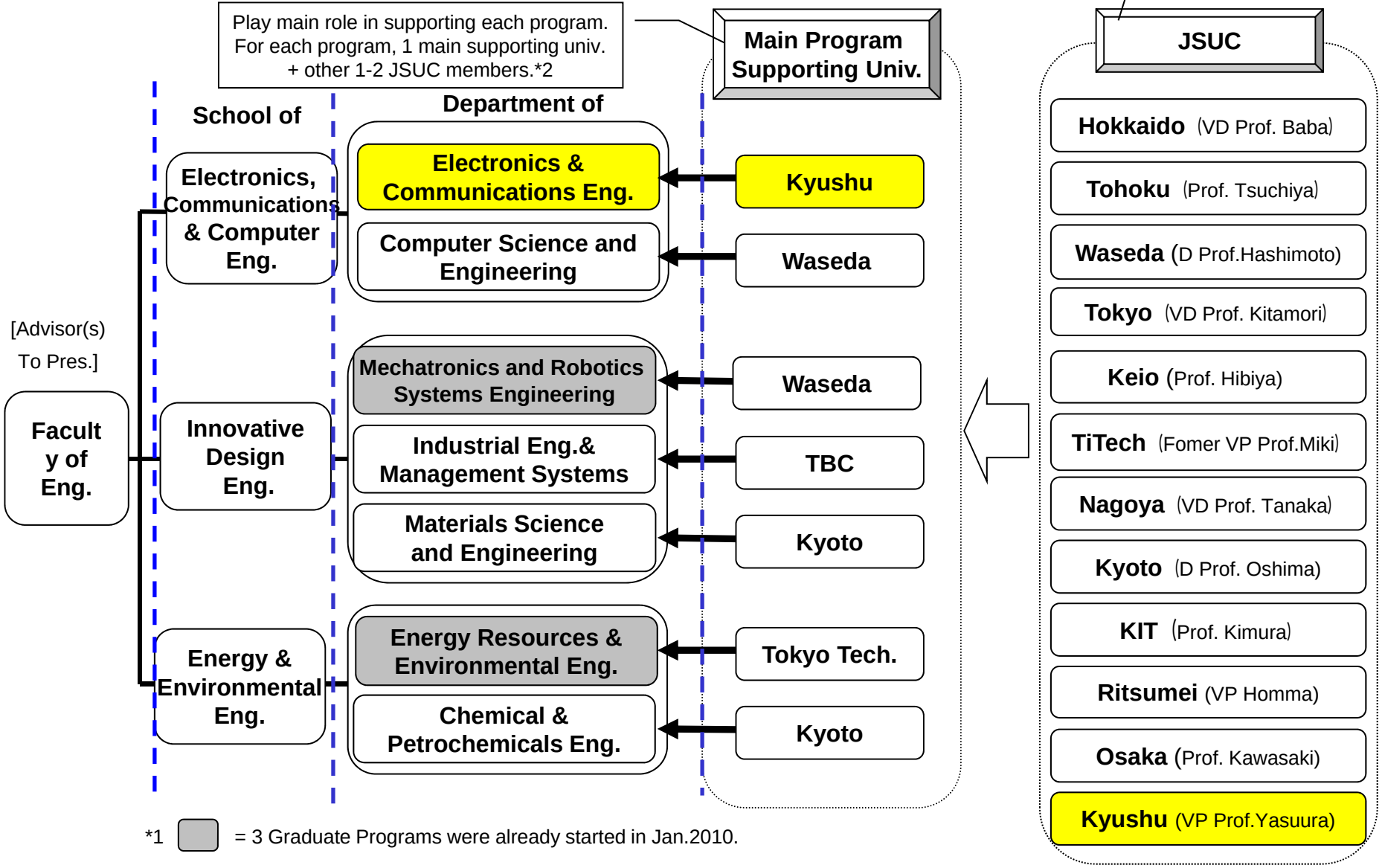
Motivation for Us (Japanese Prospect)

- First Japanese-style university abroad
  (Course system, collaborative research etc.)
- Globalization of Japanese education system in middle east and African nations
- International collaboration in science and technology

Clustering of JSUC by Programs

Chair Univ. =
Waseda (Pres.Shirai)
Kyushu (Pres.Arikawa)

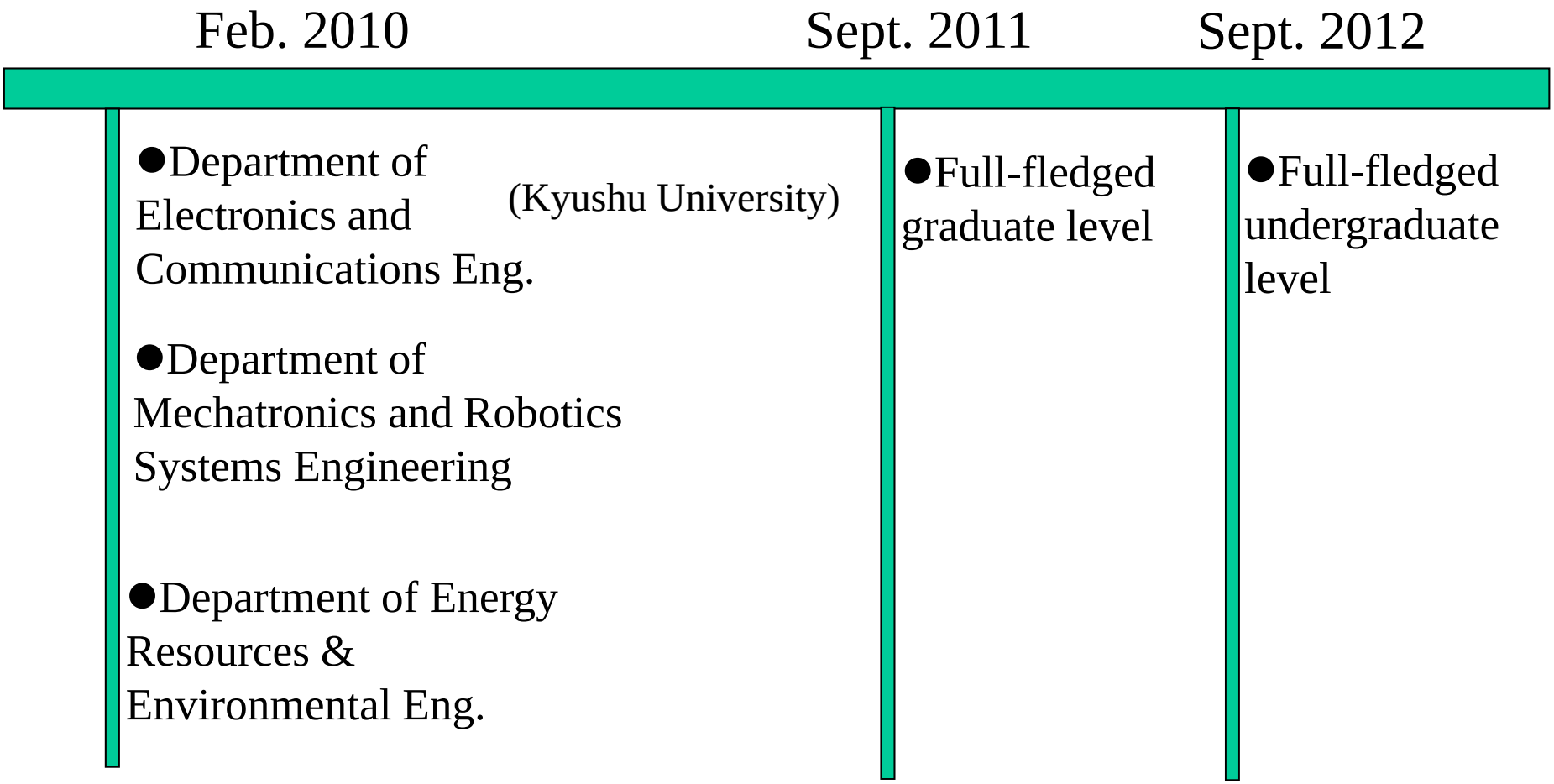
Play main role in supporting each program.
For each program, 1 main supporting univ.
+ other 1-2 JSUC members.*2



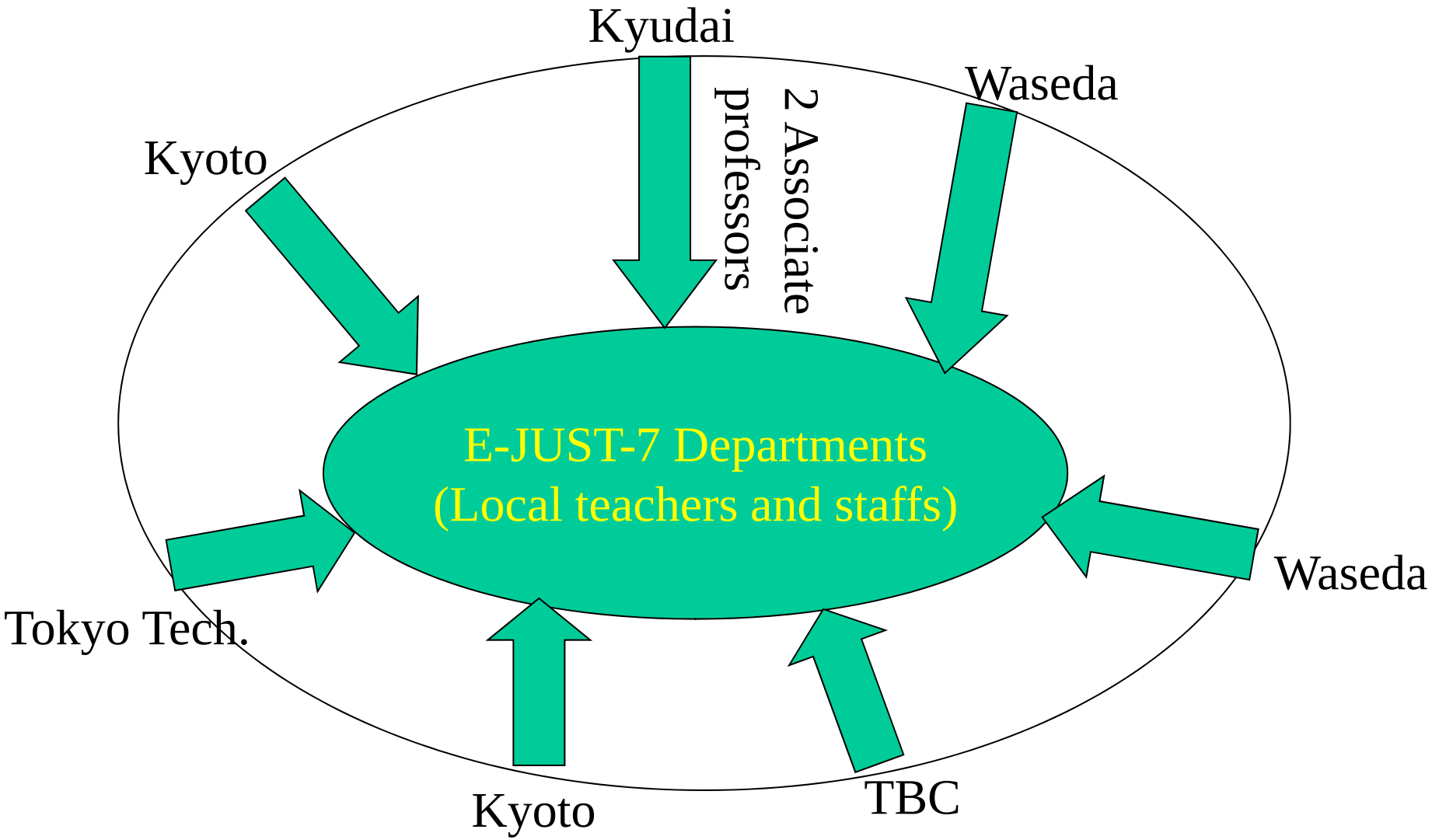
*1 = 3 Graduate Programs were already started in Jan.2010.

Kick-off Schedule

Keyword: Graduate Research Oriented Model, Among 500 Top Universities in 10 years



General Model of E-JUST and Japanese Universities (Research Supervision and Teaching Model)



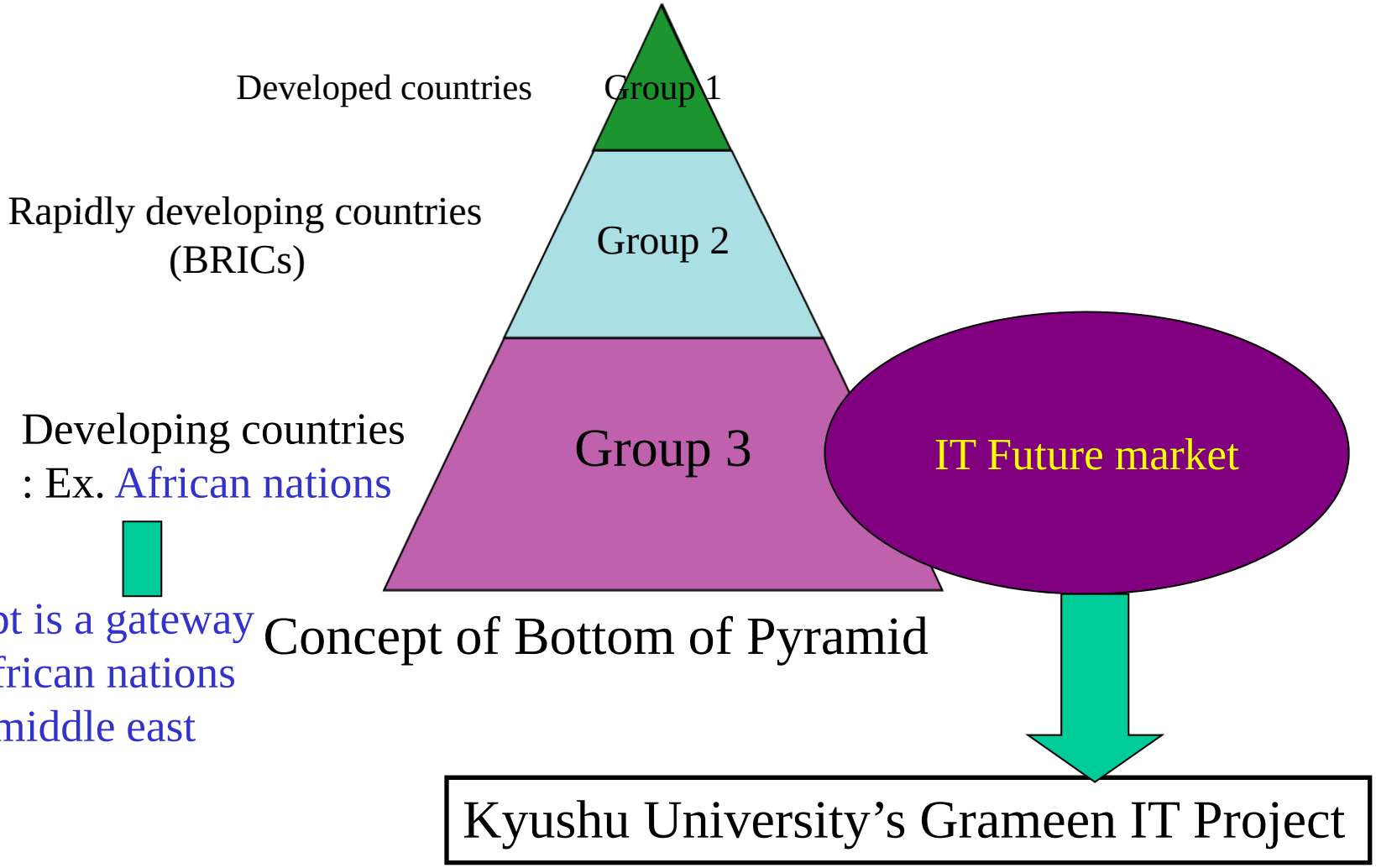
Kyudai: As an administrative body for E-JUST's Japanese Partners

- Kyudai was selected as an administrative body for E-JUST's Japanese Partners.

- How is Kyudai extending its full-fledged support to E-JUST?

Kyudai’s ongoing IT Projects and Completed IT Projects

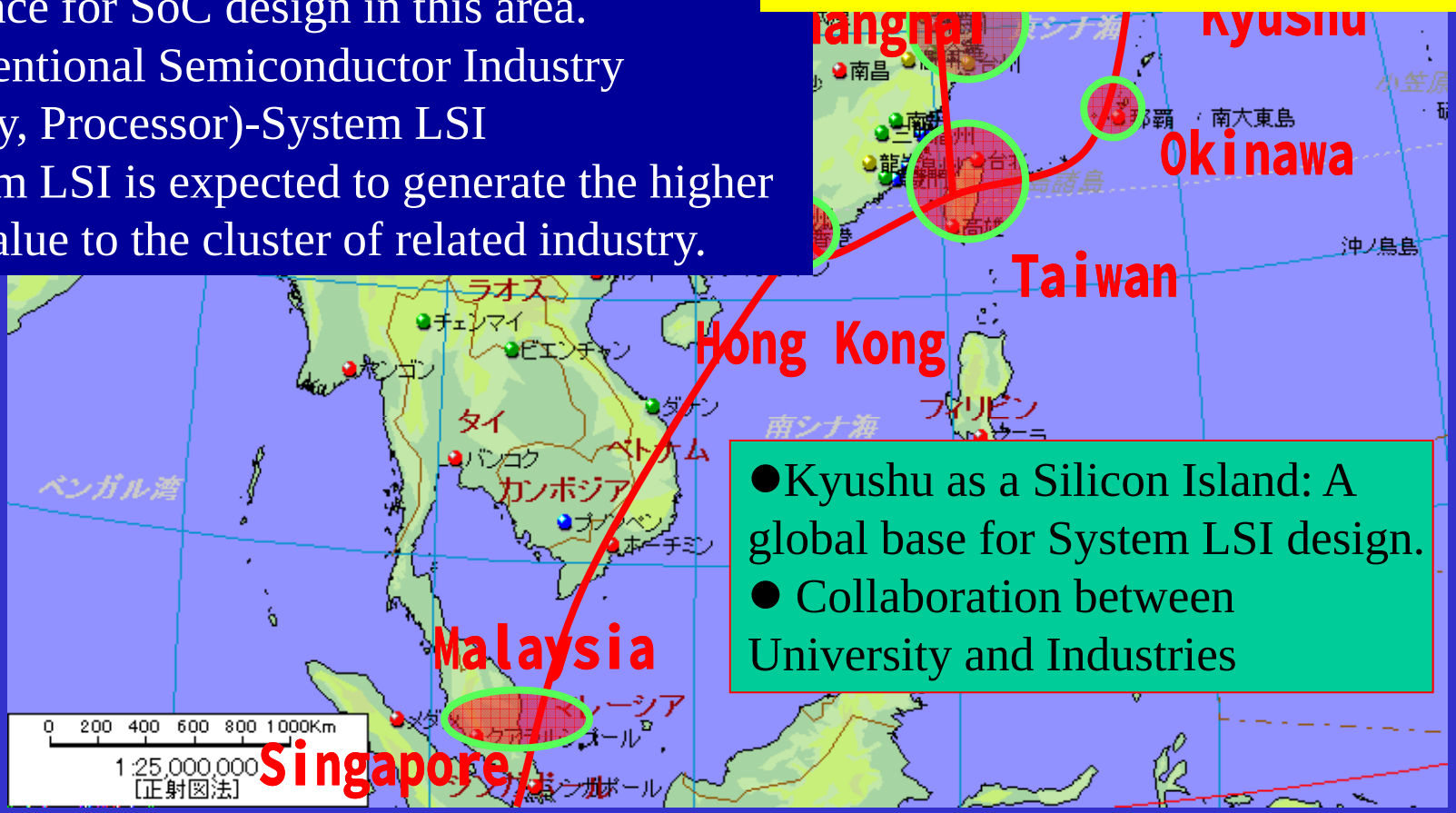
Kyudai's ongoing Rural IT Project : An example of Bangladesh (Next Presenter: Dr. Ashir)



Silicon Sea Belt Fukuoka Project: Prof. Yas

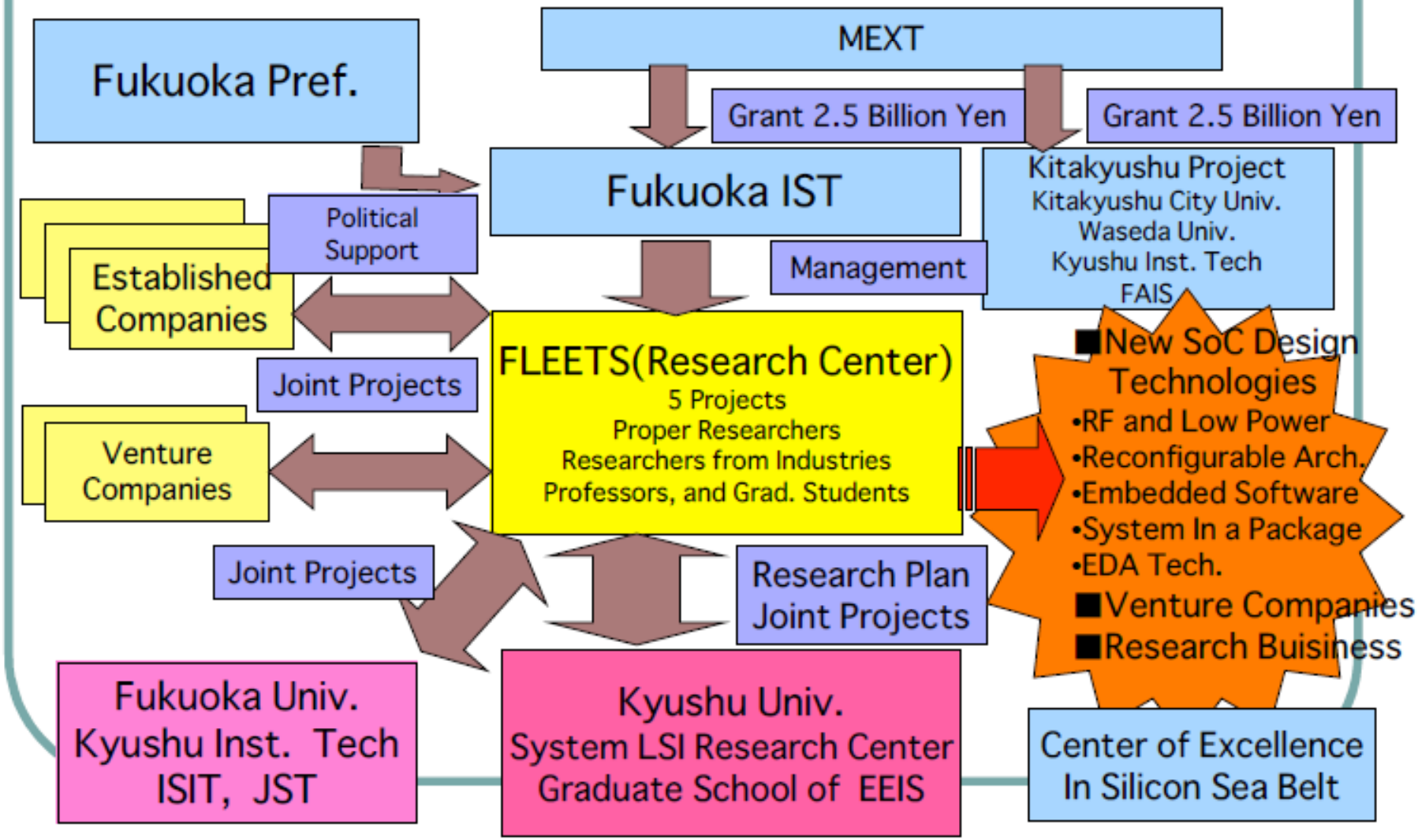
∗Center of Semiconductor design.
∗Semiconductor Industry: Driving force for th
growth.
∗ Fukuoka is addressing to establish a center o
Excellence for SoC design in this area.
∗Conventional Semiconductor Industry
(Memory, Processor)-System LSI
∗System LSI is expected to generate the higher
added value to the cluster of related industry.

Silicon Sea Belt Fukuoka Project
∗World production: 50%
∗Large consumption region



●Kyushu as a Silicon Island: A global base for System LSI design.
● Collaboration between University and Industries

CLUSS :
Innovative CLUster for Silicon Sea Belt



Research Projects in CLUSS

- Design Method for Low Energy Mobile System LSIs
  (Prof. Yoshida's group, Kyushu Univ.)
- Next Generation System LSI Architecture
  (Prof. Murakami's group, Kyushu Univ.)

} E-JUST core members

- Design Methodology for SiP (System in a Package) Module
  (Prof. Hajime Tomokage, Fukuoka Univ.)
- EDA Technology for The Next Generation
  (Prof. Yusuke Matsunaga, SLRC Kyushu Univ.)
- Design Methodology for Embedded Software
  (Prof. Akira Fukuda, Kyushu Univ.)
- Application Specific SoC Design
  (Prof. Satoshi Goto, Waseda Univ. Joint Project with Kitakyushu)

MIMO Mesh Project: A Key Enabler of Ubiquitous Broadband (Leader: Prof. Furukawa)

MIMO-MESH, Pico-MESH

Wireless backhaul Technology

Conventional MESH Device

More than 10kg
Limitation= 2~3 hubs

MESH Point

Future Image

Kyudai mesh Encryption (Lunch box)

(Open 4G system)

Battery

Drive

990g

Light

Weight

Wifi access

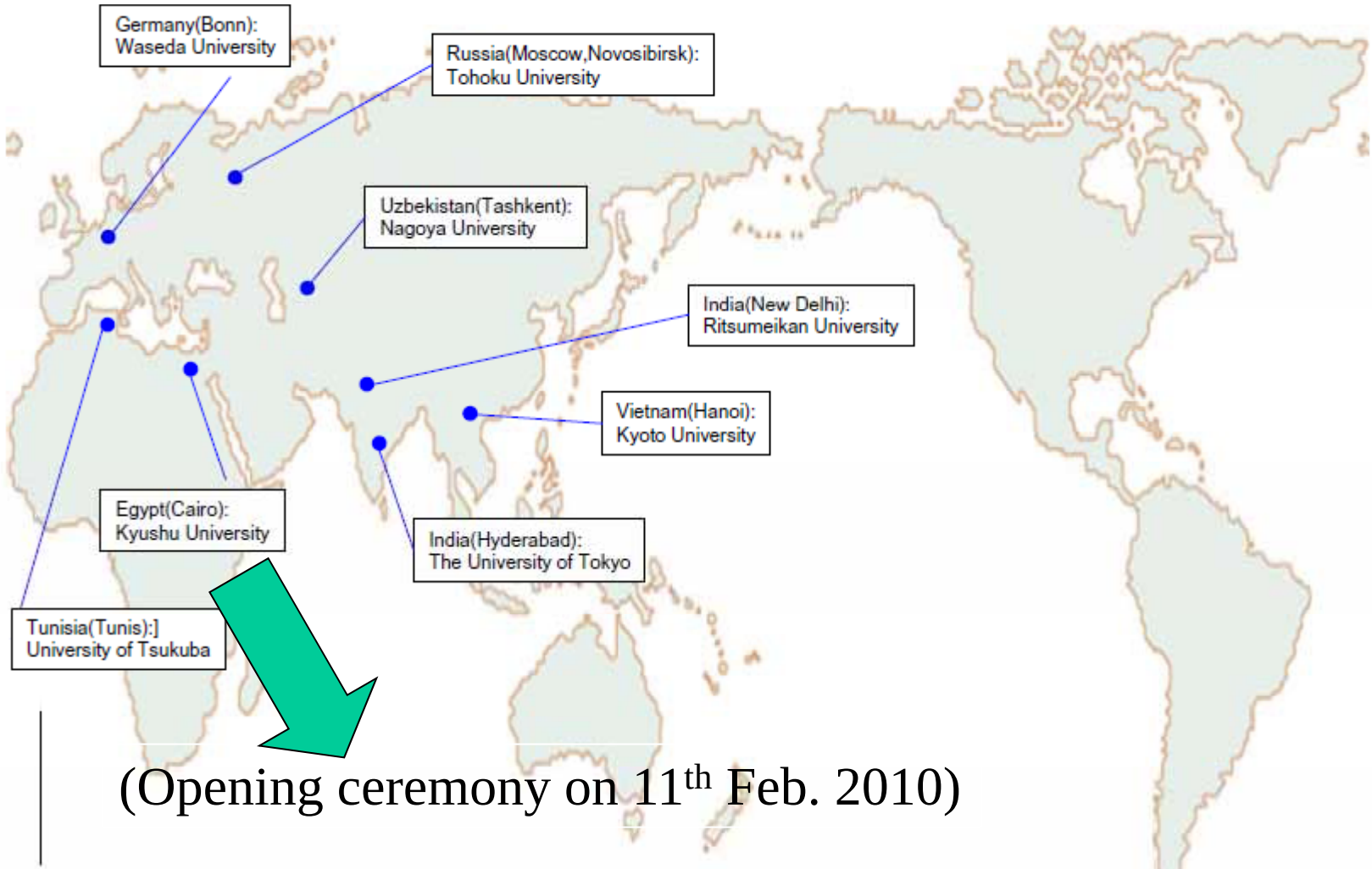
IPT

Original
frame
forwarding
Protocol

Over10hops
multihop

MEXT's Global30's Policy

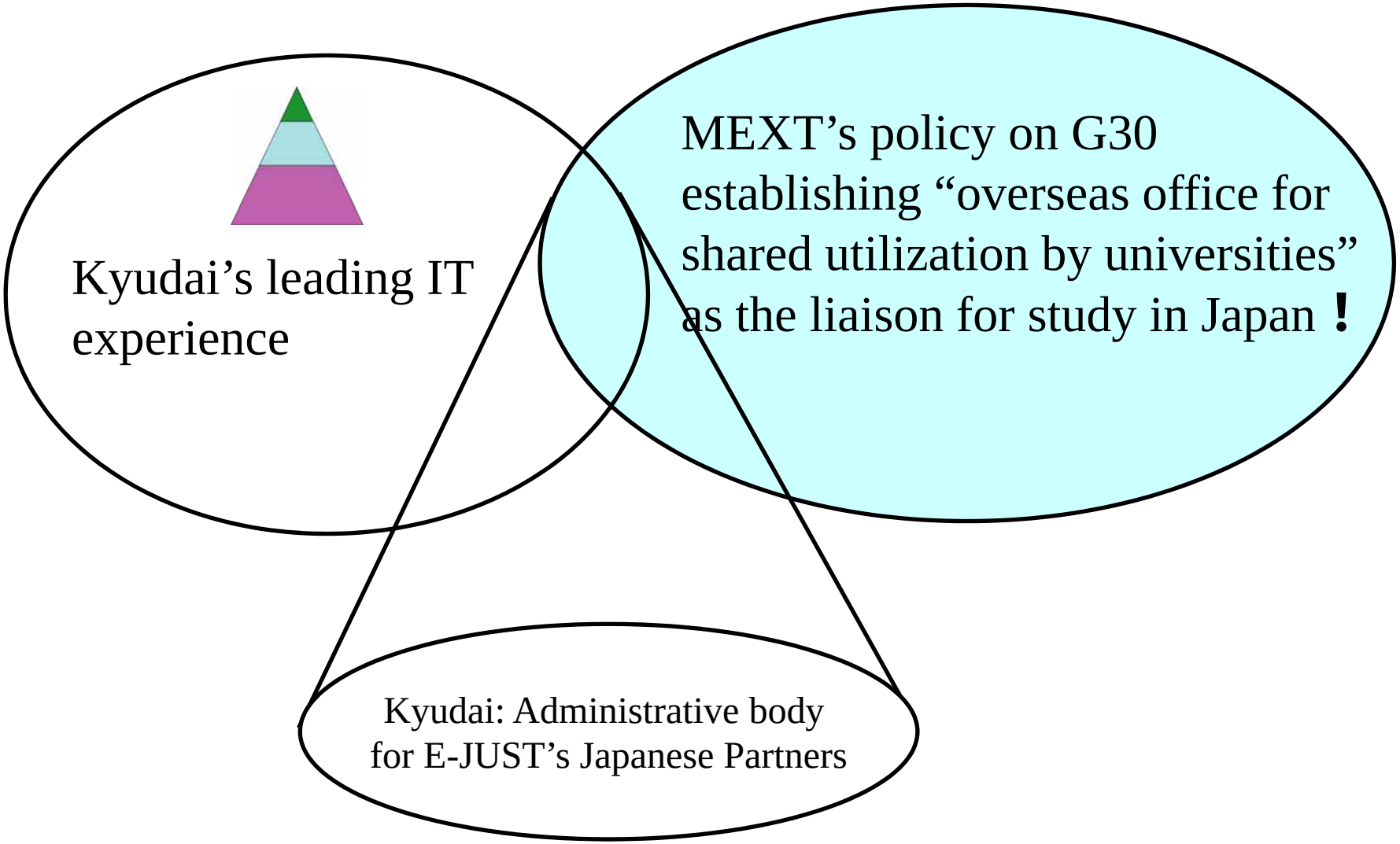
Direction to establish overseas office for shared utilization by universities



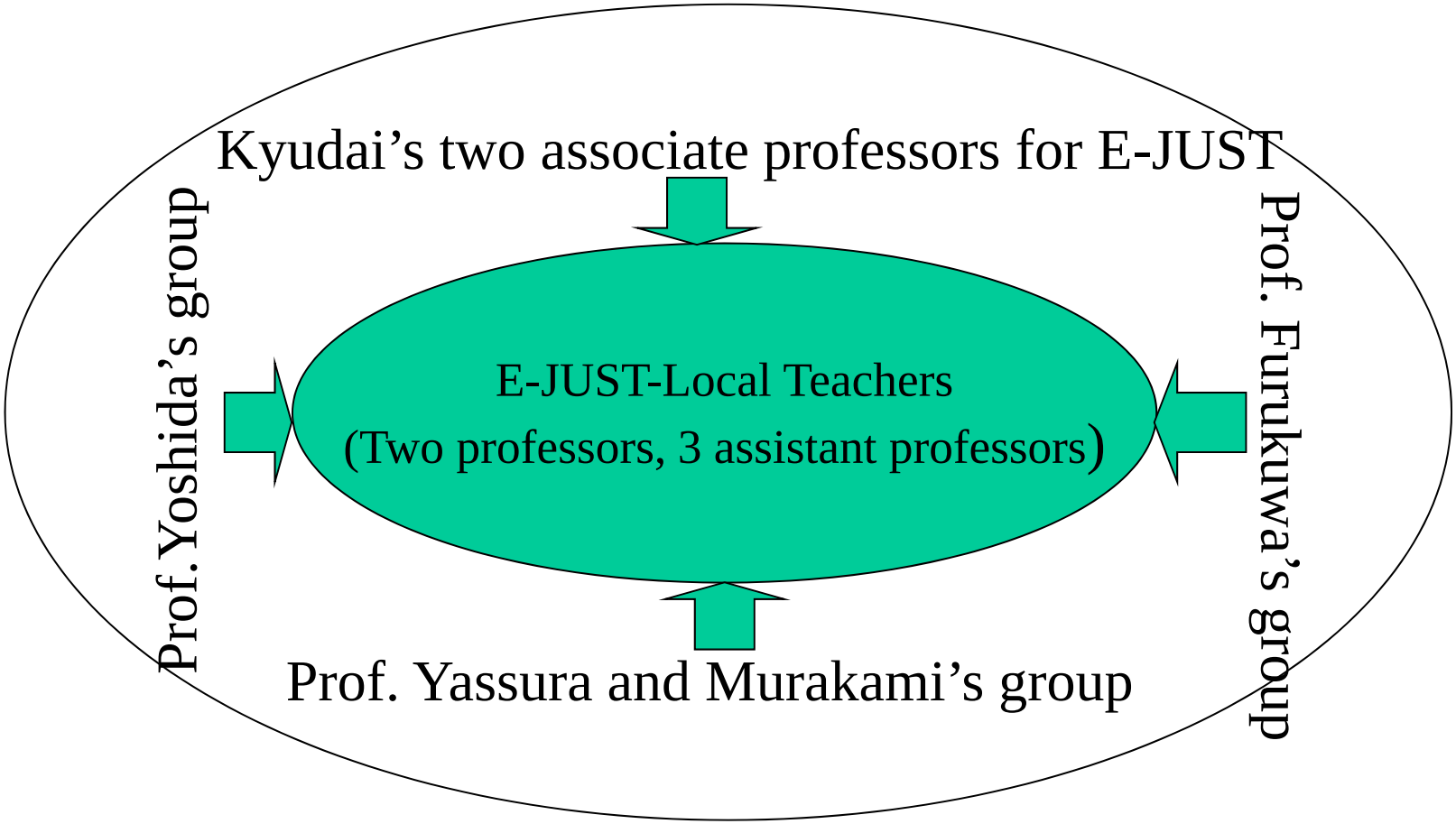
(Opening ceremony on 11th Feb. 2010)

Ref. Pic was downloaded from MEXT URL

Kyudai as an Administrative Body for E-JUST's Japanese Partners



Kyudai's model for E-JUST: A case of Department of Electronics & Communications Eng.



Two-Tier model for teaching and research supervision

Kyudai as an Administrative body for E-JUST's Japanese Partners

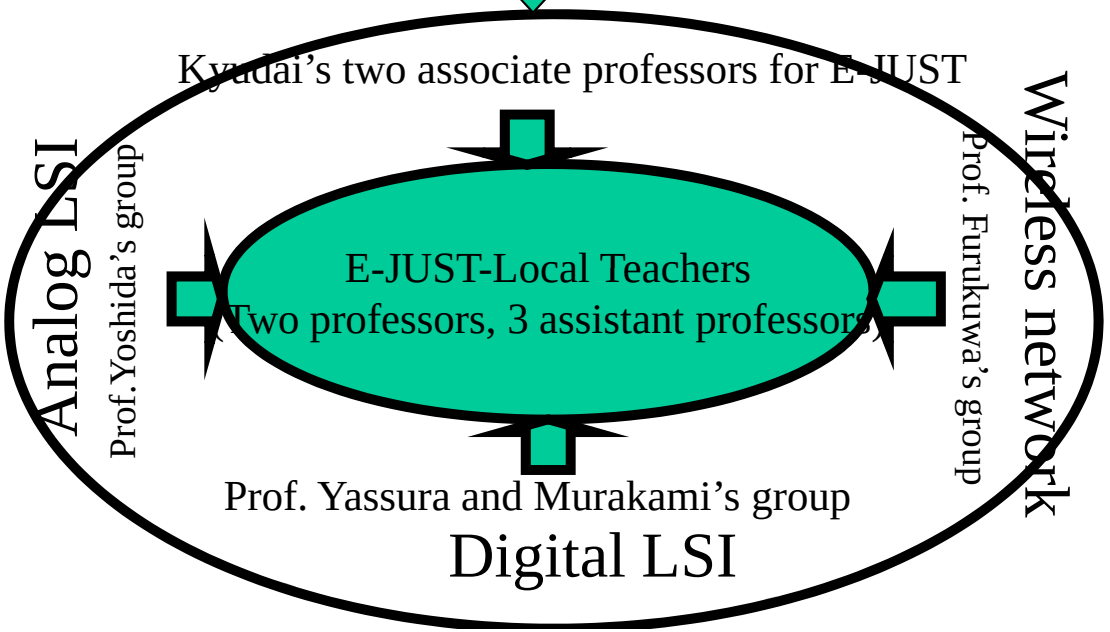
Kyushu University (All faculties)

Cooperative Center for Egypt-Japan's Science and Technology

Under Consideration

Double-degree program
(Under consideration)

●Students/Researchers exchange for collaborative research



Kyudai's Two Associate Professors for E-JUST

Stay 4.5 months at Alexandria, Egypt
and teaches the following subjects
(1) Analyses and design of VLSI
mixed signal integrated circuits (ECE 501)
(2) Advanced digital integrated circuits (ECE504)

Supervise E-JUST students directly
(in Department of Electronics and Communications Eng.)

Course Decision and Laboratory Set up : A case of DECE

A couple of round table meeting in Egypt and Japan

- Brain-storming discussion to establish a world-class syllabus
- Research Topics-State of the art laboratories

(1) Analog and radio frequency integrated circuits laboratory
(2) Digital integrated circuits laboratory
(3) Digital signal processing (DSP) laboratory
(4) Microwave engineering laboratory
(5) Center for nanotechnology (Under consideration)

Some example of close-door meetings

First round of discussion

Second round

Third round (Video conference with Prof. Murakami)

Fourth round (wrap-off meeting @Kyudai) (2009.11.07-sysllabus fixed)

Testing of CAD tools installation in E-JUST office

IC Insights top 20 rankings in 2008

Fabless Design Model still prosper for 30-40 years

2008 Top 20 Semiconductor Sales Leaders ($M)

2008 Rank	2007 Rank	Company	Headquarters	2007 Tot Semi	2008 Tot Semi	2008/2007 % Change
1	1	Intel	U.S.	35,021	34,490	-2%
2	2	Samsung	South Korea	19,951	20,272	2%
3	3	TI	U.S.	13,309	11,966	-10%
4	4	Toshiba	Japan	11,850	11,059	-7%
5	5	TSMC*	Taiwan	9,813	10,556	8%
6	7	ST**	Europe	8,637	9,052	5%
7	8	Renesas	Japan	8,001	7,017	-12%
8	13	Qualcomm***	U.S.	5,619	6,477	15%
9	9	Sony	Japan	7,203	6,420	-11%
10	6	Hynix	South Korea	9,201	6,182	-33%
11	12	Infineon	Europe	5,772	5,972	3%
12	11	AMD	U.S.	6,013	5,808	-3%
13	14	NEC	Japan	5,593	5,732	2%
14	15	Micron	U.S.	5,520	5,688	3%
15	10	NXP	Europe	6,026	5,318	-12%
16	16	Freescale	U.S.	5,447	4,898	-10%
17	23	Broadcom***	U.S.	3,754	4,509	20%
18	17	Fujitsu	Japan	4,568	4,462	-2%
19	21	Panasonic	Japan	3,810	4,321	13%
20	19	Nvidia***	U.S.	3,979	3,660	-8%
—	—	Total Top 20	—	179,087	173,859	-3%

*Foundry **Not incl. flash and ST-NXP Wireless in 2007 & 2008 ***Fabless

Source: Company reports, IC Insights

Fabless vendor

Even in the worst downturns,
Fabless company and Fabless vendor ⇒ High growth rates

IC Insights, USA

Scope & Trend

Intel (USA),
Samsung (Korea),
TI (USA) etc.

Vertically integrated (1980s)

- Owned and operated their own silicon wafer fabrication plant.
- Developed their own process technology.
- Performed assembly and test for their chips.

Technology node Running cost

EDA: CAD Tools

Collaboration

Horizontal (international) specialization

Fabless (LSI Deign)

LSI Design only, First TAT, New company, Venture company
Necessity of research and development resources for LSI Design

Foundry (LSI fabrication)

Have a deep sub-micron semiconductor fabrication
(Fabless Vendor)

Vision of DECE

Course module offered by Kyudai's two Associate professors

Analyses and design of VLSI mixed signal integrated circuits (ECE506): Project-based learning

Course outline:
Architectural and circuit level design and analysis of monolithic integrated circuits in COMS and BiCMOS technology. RF integrated electronics including LAN's, mixer, voltage controlled oscillator, and data converters (DAC and ADC). VLSI design and analysis using CAD tools. Layout optimization (Layout editor and Schematic editor), Design Rule Checker, Layout Vs. Schematic Verifier and Parasitic Extractor.

CAD tools: World-class professional tools
Attainment objectives :-
Analytical skills:
-Learn how to analyze integrated circuits using CAD tools
Practical Skills :
-Learn how to design actual electronics and how to chart them
Soft Skills:
-Master various kinds of CAD tools
Professional skills:
-Design and analyze integrated circuits in advanced CMOS and BiCOMS technology.

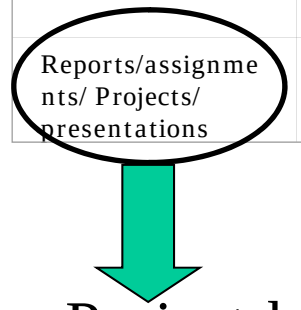
Course module offered by Kyudai's two Associate professors

Advanced digital integrated circuits (ECE504)

Week	Contents	Remarks
1	1. Overview of Digital System Design	
2	2. Fundamentals of High-Speed and Low-Power CMOS Circuits	
3	3. System-on-Chip Architecture: Overview and Applications	
4	4. System-on-Chip Components (1): Microprocessors and DSP	MIPS ISA and processor organization
5	5. System-on-Chip Components (2): Memory Systems	SRAM design tradeoff, use of CACTI
6	6. System-on-Chip Components (3): On-chip Interconnects	AMBA bus
7	7. Low-Power Design	DVS, clock gating
8	8. HDL: Verilog HDL and SystemC	Tool setup
9	9. Project Description: Microprocessor Development	FPGA-board setup
10	10. Project (1): Datapath Design and Verification	
11	11. Project (2): Control Design and Verification	
12	Project (3): Instruction Pipelining Extension	
13	Project (4): DSP Extension	
14	Project (5) : FPGA Prototyping and Evaluation	
15	Project Presentations	

Grading criteria

Kind	Percentage	Grading criteria etc.
End of semester examination	30 %	
Mid term	10 %	
Reports/assignments/ Projects/ presentations	60 %	



Project-based learning

Conclusion

- E-JUST: International Collaboration in science and technology through university
- Globalization of Japanese education system in the middle east and African nations through E-JUST.

- E-JUST-Dream come true!!!

(Within top 500 Universities in 10 years.)

Thank you for your kind attention !!