Design of Driver Circuits Connected to Transmission Line for High Speed Optical Switch

S. Nakatsuka, S. Uehara, R. K. Pokharel, H. Kanaya, and K. Yoshida

Department of Electronics, Graduate School of Information Science and Electrical Engineering, Kyushu University, Fukuoka 812-8581, Japan
E-mail: nakatsuka@yossvr3.ed.kyushu-u.ac.jp

Abstract— **For realizing high-speed and low-power-dissipated optical switches, we designed a CMOS driver circuit connected to transmission line. In order to obtain the high output voltage and low power dissipation, we designed the driver circuit by using stacked CMOS inverters. In order to transmit high-speed pulses, we studied the optimal output resistance and voltage waveforms in the transmission line. Moreover, by loading lumped inductance (*L*) in the output of the CMOS driver circuit, it is shown that we can suppress the propagation delay of this circuit from 900ps to 600ps.**

I. INTRODUCTION

"Optical switch" is the key device, which changes the route of optical signal without electro-optic conversion. In the high-speed optical communications, external optical switches using an electro-optic material $LiNbO_3$ and those using semiconductor devices have already been operated for practical use, owing to their high-speed switching characteristics [1]. There have still been great needs for realizing higher-speed and lower-power-dissipated optical switch due to increasing demands for multimedia communications. Switching times of most of today's optical switches are of millisecond order, but that of the present switch is of nanosecond order. We expect that it is used for small networks, i.e., router, rather than main networks. Fig.1 shows the schematic diagram of the optical switch, which we have been studied in our previous study [2]. The modulation voltage applied from the driver circuit must be transmitted to the open-ended transmission line.

In this paper, we study the design and the performance of the high speed driver circuit connected to the transmission line for realizing high speed optical switch. In order to realize the high output voltage, which is necessary to operate the optical switch, i.e. about 10 volts, and low power dissipation, we designed the driver circuit by using the CMOS process and stacked CMOS inverters. Because the transmission delay occurs by the impedance mismatch between output terminal of the driver circuit and the transmission line, we estimate the optimal output resistance of the driver circuit, and adjust the characteristic impedance of the transmission line. Moreover, by loading lumped inductance (L) in the output of the CMOS driver circuit, it is shown that we can suppress the propagation delay of this circuit from 900ps to 600ps.

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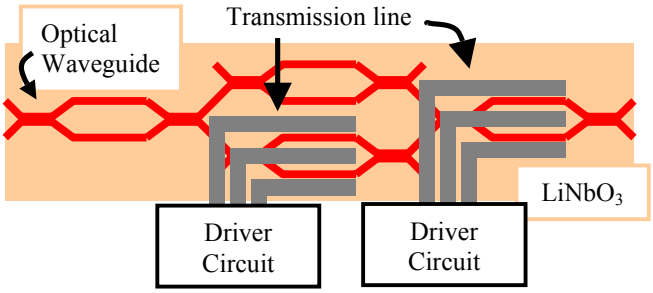

Fig.1. Schematic of the optical switch using $LiNbO_3$.

II. DESIGN OF DRIVER CIRCUIT WITH HIGH OUTPUT VOLTAGE

We adopted the CMOS inverter circuit as a core circuit, because of its low power dissipation. Fig.2 and Fig.3 show the circuit model and layout of the CMOS driver circuit. We designed and simulated the input and output characteristics by using circuit simulator ADS (Agilent technologies). The gate length is 0.25μm and V_{DD} is 4.25V. In Fig.2 and Fig.3, dotted line shows the core circuit. The total chip size of the driver circuit including DC pads is 700μm x 900μm. Because the driver circuit for optical switch must produce high voltages greater than 5 volts, it consists of differential paired CMOS inverters, and hence V_{DD} is adjusted to half of the switching voltage of the optical switch, where 8.5V was obtained in our experiment. For avoiding MOS breakdown, we stacked each nMOS and pMOS. In Fig. 2, "Out" means the output port of the driver and connected to the transmission line on the optical waveguide in $LiNbO_3$ substrate (see Fig.1).

Fig. 4 shows the time dependence of the input and output voltage at the open end of the driver circuit, namely, without load. Switching time of the current controlled driver circuit is 16ps, and power dissipation is 3W in the absence of load [3].

Switching time of the circuit we designed using a foundry (TSMC 0.25μm Mixed Signal) is 900ps, and power dissipation is almost zero at standby without load. We can realize the driver circuit with low power dissipation using CMOS inverters.

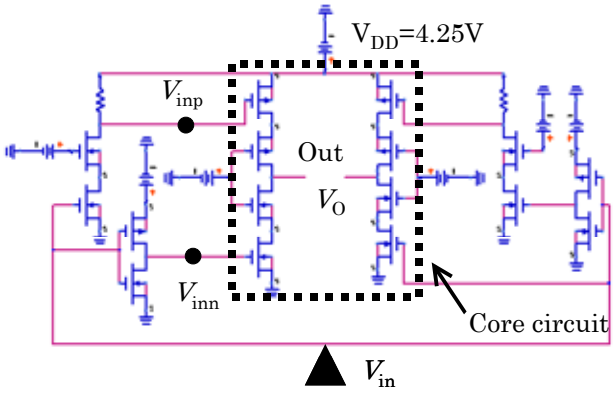

Fig.2. Circuit model of the driver circuit.

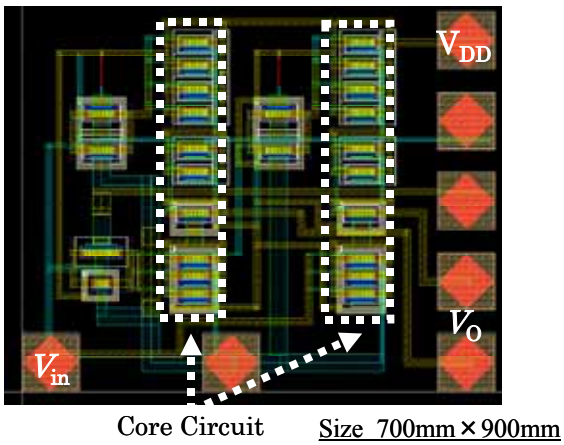

Fig.3. The layout of the driver circuit.

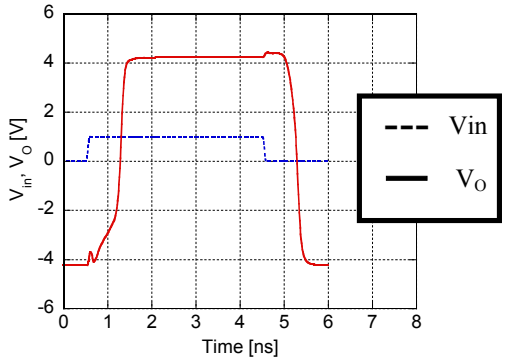

Fig.4. Time dependence of the input and output voltage at open end of the driver circuit.

The propagation delay of CMOS inverters depends on the load capacitance (C_L) and the output resistance (R_{out}) [4], where C_L mainly consists of parasitic capacitance of MOS on this circuit. C_L and R_{out} should be small values to suppress the propagation delay. However, when the gate width is increased in order to obtain the small value of R_{out}, C_L increases. To solve this problem, we propose a new method, which compensate C_L by inserting lumped inductance (L) in the output of the driver circuit. This will be explained in Chapter **III (b)**.

In the discussion below, we use "transmission delay" to denote the delay from the output port of the driver circuit to the open end of the transmission line, and "propagation delay" to denote the internal delay in the CMOS driver circuit.

III. Design of Driver Circuit for Higher Speed

a) Effects of Impedance matching between driver and transmission line

We will consider only one side of differential-pair CMOS inverters onwards. As shown in Fig.1, the output voltage from the driver circuit is given as the input to the transmission line whose other ends are open.

Fig.5 shows the circuit model of a driver circuit connecting to the transmission line. We assume the length of the line is 5 cm.

In this circuit, not only the transmission losses but also the matching condition at the termination should be extensively investigated. In order to remove the multiple reflections in the analysis, the characteristic impedance of the transmission line (Z_0) is adjusted to R_{out}, where R_{out} is explained below.

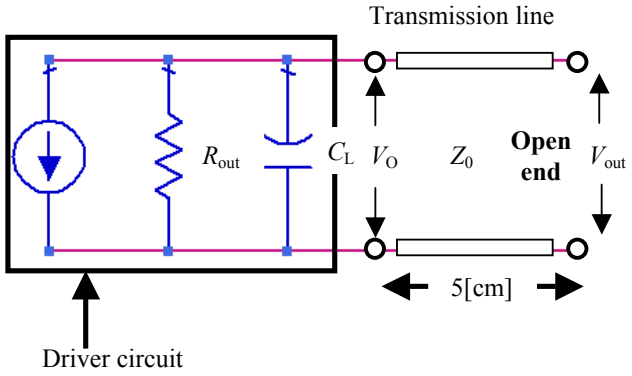

Fig.5. Circuit model connecting to the transmission line.

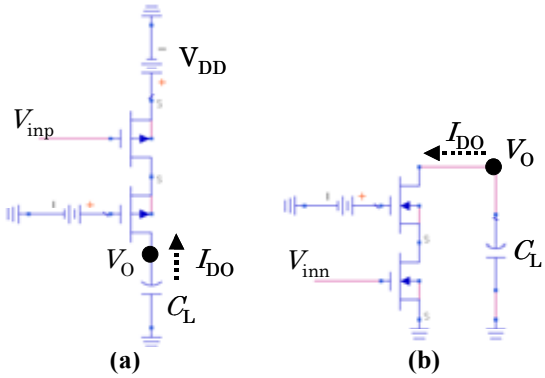

Fig.6. The equivalent circuits of the driver circuit under the 'rise' situation (a) and the 'fall' situation (b), respectively.

Fig.6 shows the equivalent circuit of the driver circuit considering two conditions of transition time. In Fig. 4, the

switching time for 'rise' condition and 'fall' condition is approximately the same. The 'rise' condition represents the switching time when voltage is increasing and the 'fall' condition represents when the voltage is decreasing. In Fig 6(a), the circuit represents 'rise' condition and that for 'fall' condition is shown in Fig. 6(b). In both circuits, R_{out} is calculated by $V_O/|I_{DO}|$, where I_{DO} is the value of the drain current at the transition point when switching of the voltage pulse starts either for the 'rise' condition or the 'fall' condition [3].

When $R_{out}=Z_0$ in Fig.5, the output voltage (V_{DD}) becomes half at the termination of the driver circuit and transmission line. The output pulse from the termination overlaps the reflected pulse from the open end of the transmission line, and thus at the open end of the transmission line, the voltage (V_{out}) thus becomes V_{DD}. In other words, the voltage on the output terminal of the driver circuit (V_O) can be considered as $V_{DD}/2$, then R_{out} becomes half ($R_{out}=V_O/|I_{DO}|=V_{DD}/2|I_{DO}|$).

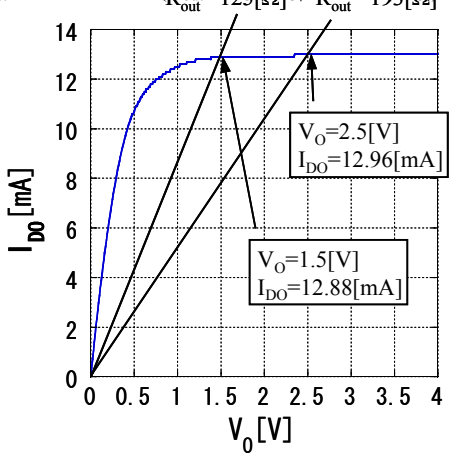

Fig.7 R_{out} on various V_{DD}.

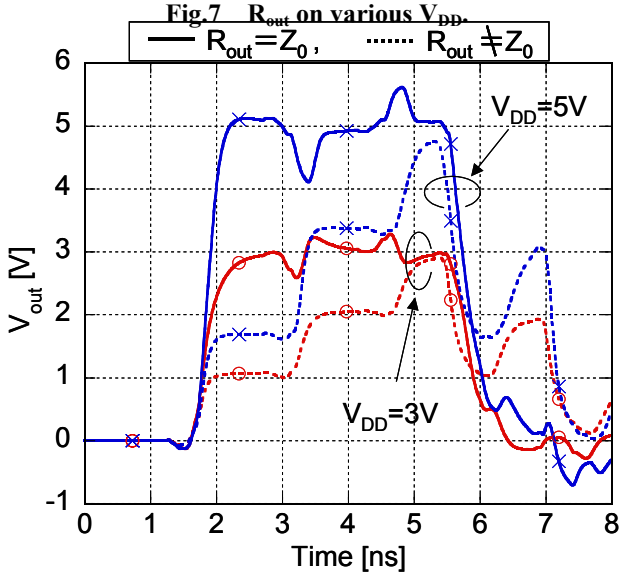

Fig.8. Time depemdence of V_{out} on various V_{DD}.

Fig.7 shows an example of estimating the value of R_{out} for two values of V_{DD}, for example V_{DD}=3.0V and V_{DD}=5.0V. Please note that this method is equally applicable for other values of V_{DD} too.

Fig.8 shows the time dependence of V_{out} assuming two terminating conditions (when $Z_0=R_{out}$ and $Z_0\neq R_{out}$). When $Z_0\neq R_{out}$, the sudden rise of the voltage pulse is dominated by the two-way round-trip time in the transmission line and the magnitude is also doubled on the arrival of the first reflected wave. These procedures are examined for various conditions of V_{DD} and the tendency becomes the same for each value. Therefore, the graphs for only two values of V_{DD} (V_{DD}=3V and V_{DD}=5.0V) are illustrated in the figure.

Furthermore, when $Z_0=R_{out}$, the effect of multiple reflections has been greatly suppressed. However, even when $Z_0=R_{out}$, the small ripples are still present. These are attributed to the mismatch in the imaginary part of Z_0 that is contributed by C_L.

In order to mitigate this problem, we will here propose a method to compensate it by inserting a lumped inductor (L) in the output of the driver circuit. By inserting a lumped inductor, we can suppress not only these ripples but also the propagation delay which will be discussed in the next section.

b) Speedup by inductance loading

As mentioned in Chapter **II**, the propagation delay of CMOS inverters depends on $R_{out}C_L$. When the gate width is increased in order to obtain the small value of R_{out}, C_L is increased. To solve this problem, we proposed a new method, which compensates C_L by inserting lumped inductance (L) in the output of the driver circuit and the circuit that consists of the compensating inductance, L and the C_L is depicted in Fig. 9.

Fig.10 shows the time dependence of V_{out} on various L, where the ripples are suppressed with the increase of L within certain limit, and 10nH of L is the optimum value obtained from the analysis. Fig.11 is an enlargement version of Fig.10 in order to observe the influence of L during switching time. In the figure, it is noted that the propagation delay when L is 10nH is 600ps. Through out this paper, the propagation delay is defined as the time required for V_{out} to reach $0.9V_{DD}$.

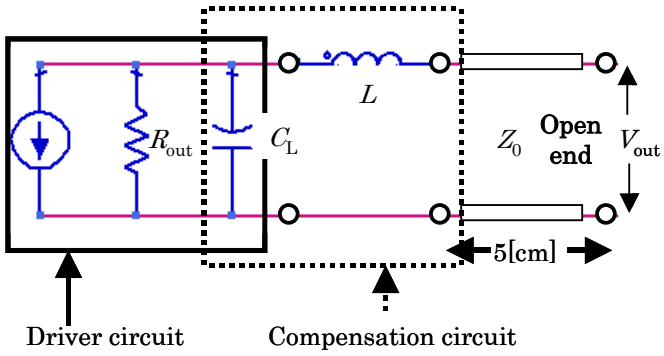

Fig.9. Circuit model of inserting lumped inductor (L).

In order to realize such high value of the lumped inductance by TSMC CMOS process, it is necessary to investigate the process using either a spiral inductor or meander inductor or bonding wire or by compensation of the input impedance by changing the width of the line at the input terminal, and this is

taken as one of our priority works in the near future.

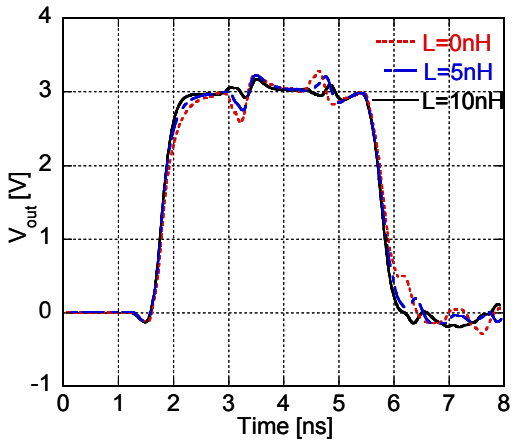

Fig.10. Time dependence of V_{out} on various *L*.

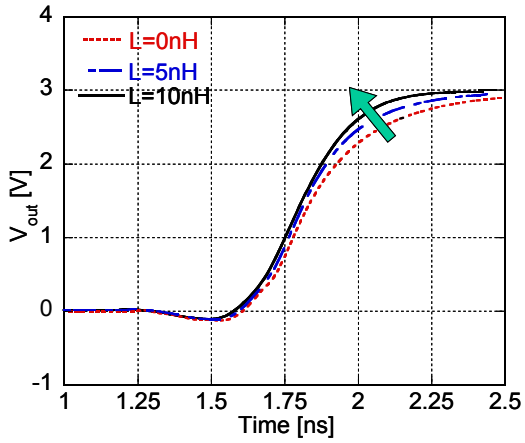

Fig.11. Enlargement version of Fig.10.

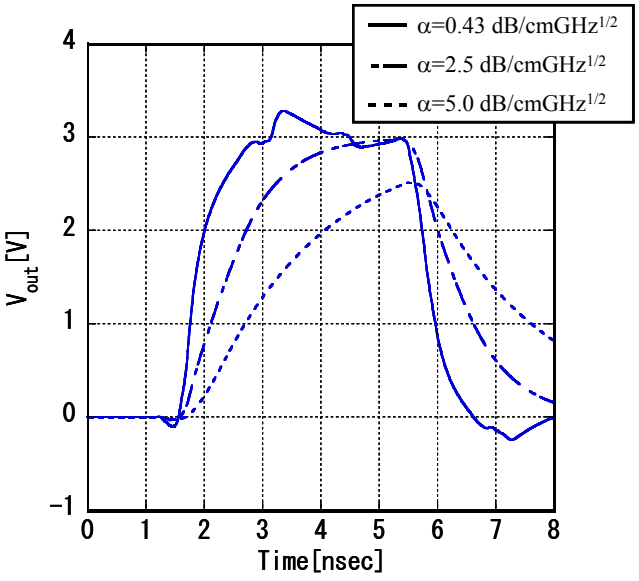

Fig.12. Time dependence of V_{out} on various α.

IV. Effect of Electrode Loss of Transmission Line

We mentioned above the transmission line has no loss. But we will mention the transmission line has some loss.

Fig.12 shows the time dependence of V_{out} on various α. α is the attenuation constant of the transmission line.

As Fig.12 shows, if the transmission line has some loss, it enlarges the transmission delay. In order to transmit high-speed pulses, the loss of the metal transmission line should be suppressed. We can obtain the small attenuation constants, α=0.43dB/cmGHz$^{1/2}$, using thick Au [5].

V. Conclusions

We have carried out the theoretical investigation on the high-voltage and low-power-dissipated driver circuit. Based on the analysis, a method in order to compensate C_L by inserting lumped inductance (L) at the output of the driver circuit is presented. By this method, not only the matching of the circuit can be realized but also propagation delay can be improved. This method is effective not only in CMOS inverter circuits, but also equally applicable in general digital circuits too.

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