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Design of Coplanar Waveguide Matching Circuit for RF-CMOS Front-End

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SUMMARY

For enhanced performance with smaller transceiver size at microwave frequencies, a design method is proposed in which the impedance matching network is included in the filter and integrated with the antenna. In this paper, a low noise amplifier (LNA) and a power amplifier (PA) are designed by the CMOS process. A method is presented in which the input and output impedances are matched on the chip by a matching circuit using distributed transmission lines. As the distributed transmission lines, coplanar waveguides (CPW) are used for realization of miniaturized design. First, the RF characteristics of the CPW meander line are evaluated by an electromagnetic field simulator and are compared with measured results. Next, an amplifier integrated with matching circuits is designed and its performance is predicted by a simulator. The targeted frequency of operation is 2.4 GHz for wireless LAN (IEEE802.11b). © 2005 Wiley Periodicals, Inc. Electron Comm Jpn Pt 2, 88(7): 19–26, 2005; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/ecjb.20161

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Key words: RF-CMOS; wireless LAN; coplanar waveguide; impedance matching circuit.

1. Introduction

With the rapid development of the information society represented by mobile communications (IMT2000), wireless LAN, and satellite communications, the development of devices to realize communications systems with higher performance and higher efficiency is necessary. In order to meet this need, it is an urgent task to develop monolithic microwave integrated circuits (MMIC) in which filters, low-noise amplifiers (LNA), and power amplifiers (PA), as well as base band circuits and digital circuits, are integrated by applying CMOS circuits, with good digital circuit compatibility, to analog circuits [1, 2]. Already in wireless LAN, a two-chip system has been developed for RF front ends for PC cards. However, the frequency selection filter and the harmonic rejection filter are externally installed.

Also, for 50-Ω matching (conjugate matching) and noise matching with external circuits, spiral inductors are mounted on a CMOS chip in the case of low-noise amplifiers. But their size prevents miniaturized design. Further, since the spiral inductor has an extremely low Q and may have self-resonance, it is difficult to operate at higher frequencies with high gain and low noise. Also, filter design is not possible.

As a design method eliminating the spiral inductor for future higher frequency operations, the authors have introduced a resonator configuration using a distributed

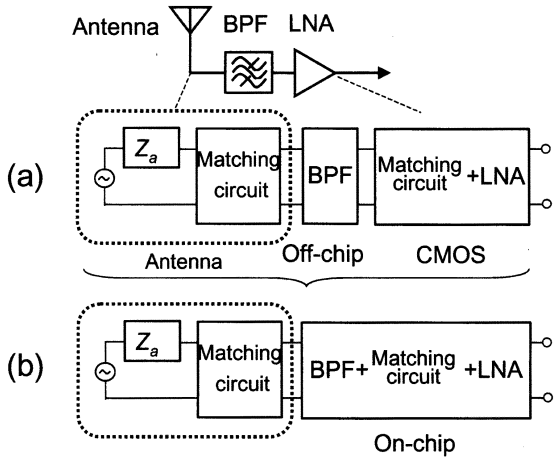

Fig. 1. Block diagram of the RF section.
(a) Conventional type. (b) On-chip type.

transmission line and an impedance inverter (inverter circuit). It is planned to realize on CMOS a circuit element combining a filter (bandpass design) and a matching circuit. The size of the distributed resonator can be reduced in inverse proportion to the frequency.

Since the coplanar waveguide (CPW) is used as a transmission line in which the signal line and the grounding conductors are on the same plane, coupling with CMOS active devices is easy and grounding is also simple. Hence, miniaturization of the devices is possible. Figure 1 shows a block diagram of the RF section. In the usual system, the filter is connected externally as shown in panel (a). The present authors have designed and published an antenna integrated with a filter in which the antenna, matching circuit, and filter are integrated together [3–5]. In the present research, a filter is designed on CMOS as shown in panel (b). The objective is to unify the input and output matching networks with the filter. The 2.4-GHz band used for wireless LAN (IEEE802.11b) is the targeted frequency.

2. Design Method for Matching Circuits

The present matching circuit is based on the theory of the Chebyshev bandpass filter (BPF) [6]. The BPF consists of distributed transmission lines and impedance inverters (K inverters, $K_{i,i+1}$). In usual wireless LAN cards, a chip dielectric filter is used as an external BPF. Its specifications are usually a passband of 100 MHz, an insertion loss of 1.5 dB, 0.5-dB Chebyshev ripple, and an attenuation of 30 dB at 1.9 GHz. In order to meet these specifications, at least a three-stage BPF characteristic is needed. It is desirable to improve selectivity by increasing the number of stages in the BPF. Due to limited chip area, this paper uses a one-stage filter. The design formula for a one-stage BPF using the impedance inverters (K inverters) shown in Fig. 2 is

$$K_{0,1} = \sqrt{w}\sqrt{\frac{Z_0 x_1}{g_0 g_1}} \tag{1}$$

$$K_{1,2} = \sqrt{w}\sqrt{\frac{x_1 Z_0}{g_1 g_2}} \tag{2}$$

$$X_1 = x_1\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) \tag{3}$$

Here, X_1 is the reactance in the series resonator with a reactance slope parameter x_1, w is the relative bandwidth, and g_i is the filter parameter.

The equivalent circuit of the filter in Fig. 2 at the center part is shown in Fig. 3. Hence, the resistance ratio and the Q value are given by

$$\frac{R'_L}{R'_S} = \frac{g_0}{g_2} \tag{4}$$

$$Q = \frac{x_1}{R'_S + R'_L} = \frac{g_0 g_1 g_2}{w\,(g_0 + g_2)} \tag{5}$$

Next, let us explain a miniaturization design method using a λ/4 transmission line.

Figure 4 shows a new distributed impedance matching circuit proposed by the present authors using a K inverter and a λ/4 transmission line. Since the same design method can be used for both the input and output sides, only the input matching circuit is described. Here Y_L is the input admittance of the LNA and is given by

$$Y_L = \frac{1}{Z_L} \equiv G_L + jB_L \tag{6}$$

In the compensation circuit, Δl is determined by Eq. (7) in such a way that the susceptance B_L of the LNA is canceled. Here, C (F/m) is the capacitance per unit length of the distributed transmission line:

$$\Delta l = -\frac{B_L}{\omega_0 C} \tag{7}$$

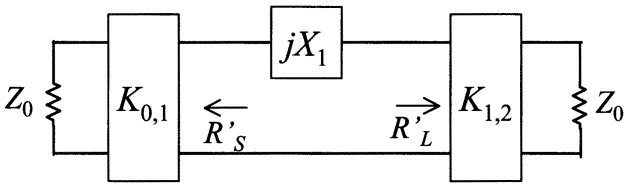

Fig. 2. Circuit model of the one-pole BPF with K inverter.

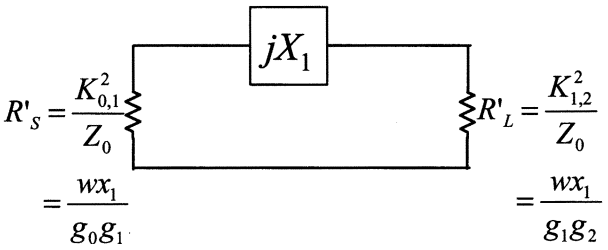

Fig. 3. Equivalent circuit model at center frequency.

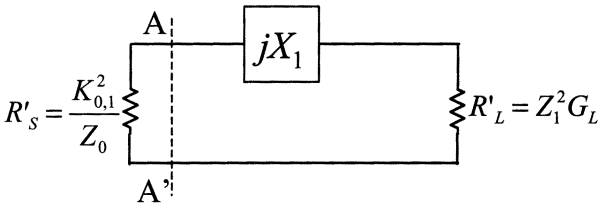

Fig. 5. Equivalent circuit model at A–A′ in Fig. 4.

Next, in Fig. 4, Z'_L and R'_S can be written in terms of the characteristic impedance Z_1 and the electrical length θ of the λ/4 transmission line as follows:

$$Z'_L = Z_1^2 G_L + jX_1 \equiv R'_L + jX'_L \tag{8}$$

$$X_1 = -Z_1 \cot\theta \cong x_1 \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \tag{9}$$

$$x'_1 = \frac{\pi}{4} Z_1 \tag{10}$$

$$R'_L = Z_1^2 G_L \tag{11}$$

$$R'_S = \frac{K_{0,1}^2}{Z_0} \tag{12}$$

It is assumed in Eq. (8) that the input impedance of the LNA is sufficiently larger than Z_0 so that $|Y_L| << Y_0$. Hence, the equivalent circuit at A–A′ can be modified to that in Fig. 5.

To make this structure identical to the one-stage filter, it is found from resonant conditions (4) and (5) that

$$\frac{R'_L}{R'_S} = \frac{Z_0}{K_{0,1}^2} Z_1^2 G_L = \frac{g_0}{g_2} \tag{13}$$

$$Q = \frac{x_1}{R'_S + R'_L} = \frac{Z_0}{K_{0,1}^2} \frac{x_1}{\left(1 + \frac{g_0}{g_2}\right)} = \frac{g_0 g_1 g_2}{w\,(g_0 + g_2)} \tag{14}$$

When these two equations are solved for $K_{0,1}$ and Z_1, the following are eventually obtained as design formulas:

$$Z_1 = \frac{\pi}{4} \frac{w}{g_1 g_2 G_L} \tag{15}$$

$$K_{0,1} = \sqrt{w} \sqrt{\frac{Z_0 x_1}{g_0 g_1}} \tag{16}$$

$$x_1 = \frac{\pi}{4} Z_1 \tag{17}$$

Therefore, impedance matching is possible with the characteristic impedance (Z_1) of the λ/4 transmission line and $K_{0,1}$. Also, it is found from Eq. (16) that the desired bandwidth can be obtained by varying w. If noise matching is used, the above can also be applied by letting $Y_L = Y_{opt}^*$ (Y_{opt} is the admittance minimizing the noise) [7].

3. Design of Matching Circuit

For microwave circuits, microstrip lines are often used. In order to design the matching circuit on CMOS, the present authors use coplanar waveguides (CPW). As shown in Fig. 6, CPW can realize grounding easily since the signal line and the grounding conductors are on the same plane. In addition, the characteristic impedance of the transmission line can be determined from the ratio of the signal line width and the ground plane separation. Hence, miniaturiza-

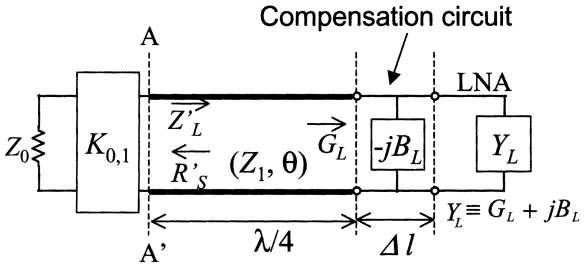

Fig. 4. Circuit model of the quarter-wavelength matching circuit.

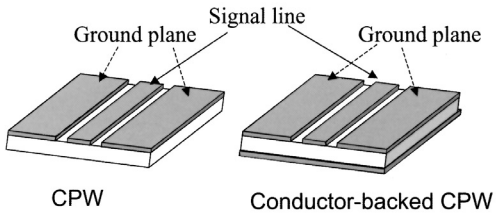

Fig. 6. Schematic diagram of the CPW structure.

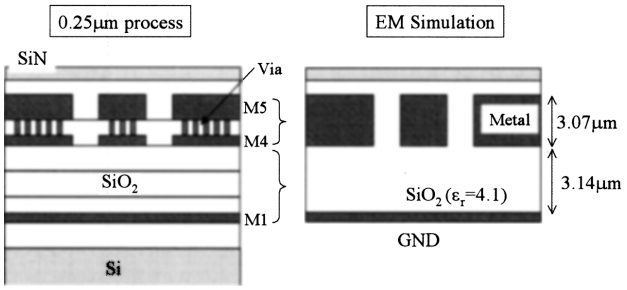

Fig. 7. Sectional views of the real process and EM-simulated condition.

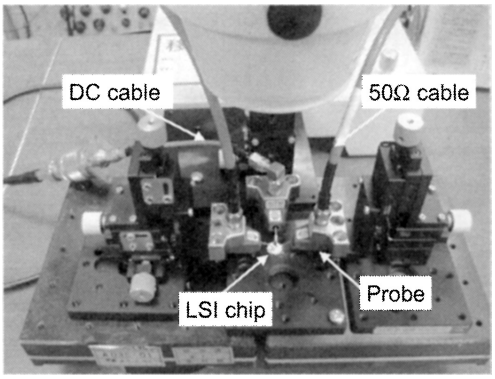

Fig. 9. Photograph of the RF measuring system.

tion is possible by proportional size reduction. Also, in comparison with microstrip lines, the electric field emissions are smaller, so that coupling to other circuits can be reduced. Further, in order to eliminate the influence of losses in the Si substrate, a conductor-backed CPW is used, combining the lowest level metallization (see Fig. 6). The Momentum simulator (Agilent Technology) is used for electromagnetic field simulation of the CPW.

Figure 7 shows a cross-sectional view of the substrate modeled in the electromagnetic field simulation. In order to reduce metal loss, metal layer 5 and metal layer 4 are connected with many vias. Note that the conductors are Al and the dielectric is SiO_2. Simulations are performed using the physical constants for conductivity, permittivity, and dielectric dissipation. Figure 8 shows the layout image of the CPW matching circuit. As shown in Fig. 8, meander line configurations are used for the λ/4 transmission line and the compensation circuit for miniaturization. A meander short stub is used as a *K* inverter.

4. Design of Matching Circuit

Figure 9 shows a photograph of the measurement system for RF transmission characteristics. For measurement, air coplanar probes (Cascade Microtech) are used. As a preliminary experiment, a test chip with a 50-Ω transmission line is evaluated prior to evaluation of the conductor-backed CPW. Figure 10 shows a chip photograph. The signal line width is 10 μm. The transmission line has a meander shape with a length of 13 mm. The line length corresponds to a λ/4 transmission line at 2.45 GHz. Figure 11 shows the measured results. For comparison, the simulation results obtained with the electromagnetic field simulator are also plotted. From the results of the electromagnetic field simulation, it is anticipated that attenuation of about 1 dB is possible near 2.45 GHz due to loss of the aluminum electrode (electrode loss). On the other hand, in the experiment, an additional loss of 1 dB is seen in the experimental results. This is attributed to loss by the measurement PAD (including the connection with the coplanar probe). However, since the agreement with the results of the electromagnetic field simulator is reasonable, it is found that CPW design by the electromagnetic field simulator is possible. In the future, an increase of the operating frequency for improved communications speed is conceivable. Therefore, further miniaturization and loss reduction will be possible by means of reduced transmission line length.

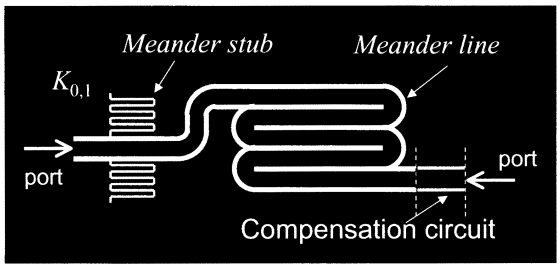

Fig. 8. Layout image of the CPW matching circuit.

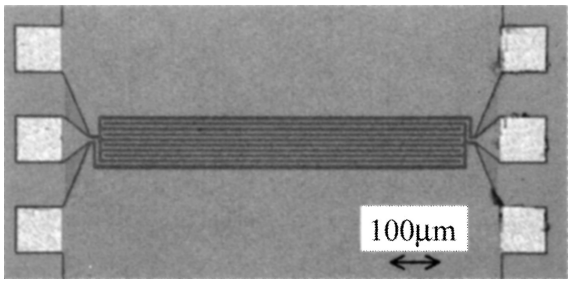

Fig. 10. Photograph of the conductor-backed CPW.

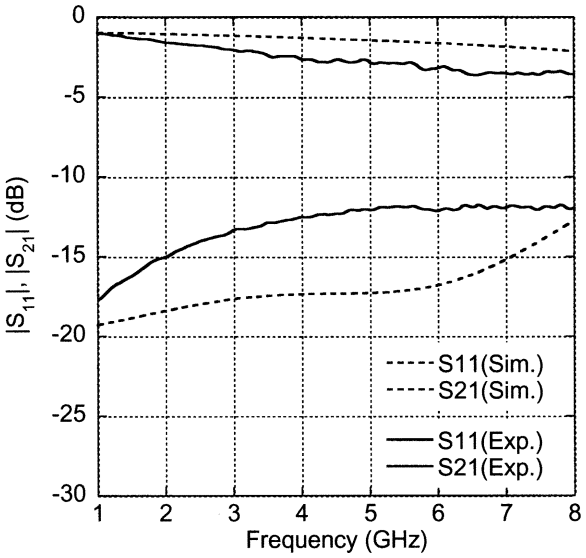

Fig. 11. Characteristics of the conductor-backed CPW.

5. Design of LNA Integrated with a Matching Circuit

Although design was carried out for both LNA and PA, only the design for the LNA is described here. In the design of the LNA, the 0.25-μm CMOS process with TSMC is used. As the CAD tool, Virtuoso (Cadence) provided by VDEC is used. Also, for calculation of the input and output impedances and the noise figure of the LNA, ADS (by Agilent Technology) is used. Since an RF front end for the wireless LAN (for IEEE802.11b) is designed, a center frequency of 2.447 GHz and a bandwidth of 100 MHz are chosen. The input and output matching circuits using the K inverters and a λ/4 transmission line are designed. The design theory is verified by means of electromagnetic field simulation.

First, the input and output impedances of the LNA at 2.45 GHz are measured by the circuit simulator. Next, by using the obtained input and output impedance values, the matching circuit is designed by means of the electromagnetic field simulator. In the design, the port impedance of the electromagnetic field simulator is replaced by the input or output impedance of the LNA. The S parameters of the matching circuit section obtained by the electromagnetic field simulator are entered into the circuit simulator and the final results are obtained by combining them with the amplifier section. Figure 12 shows a chip layout of the LNA with an attached matching circuit integrated with a one-stage filter as the input and output. For size reduction, a meander configuration with undulating transmission lines as shown in Fig. 10 is used. At the input and output sections, CPW pads are installed for measurement by the air coplanar probe. The area occupied by the amplifier section is 2.2 × 0.2 mm including the input and output pads.

Figure 13 shows the frequency characteristics of the input power gain and the reflection coefficient. In the simulation results, the loss of the aluminum electrodes is taken into account but not the loss of the CPW obtained in the experiment. From the circuit simulation, the power gain is 15 dB at 2.45 GHz. From the reflection coefficient in Fig. 13, matching around 2.45 GHz is obvious. Also, as shown in Fig. 14, the noise figure of 1.8 dB is obtained at 2.45 GHz. In Fig. 15, the input and output impedances at the

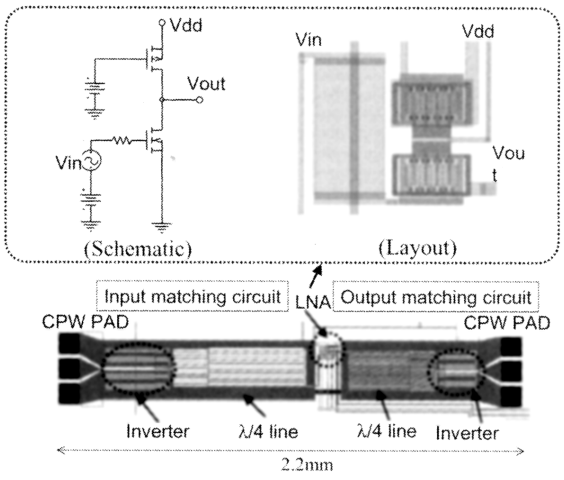

Fig. 12. Layout of input and output matching circuit connected with LNA.

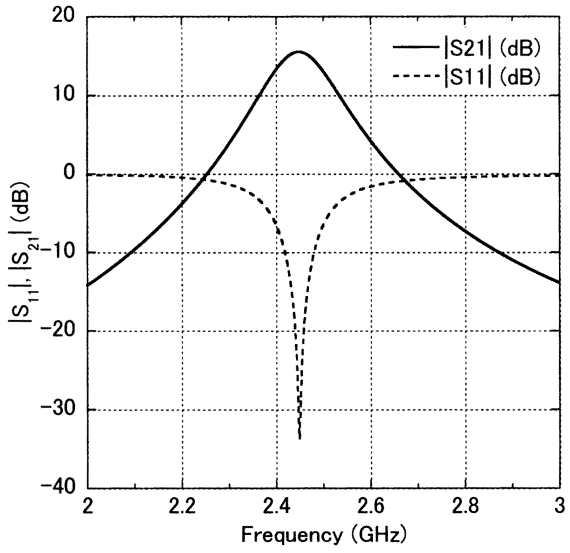

Fig. 13. Characteristics of the LNA with input and output matching circuit.

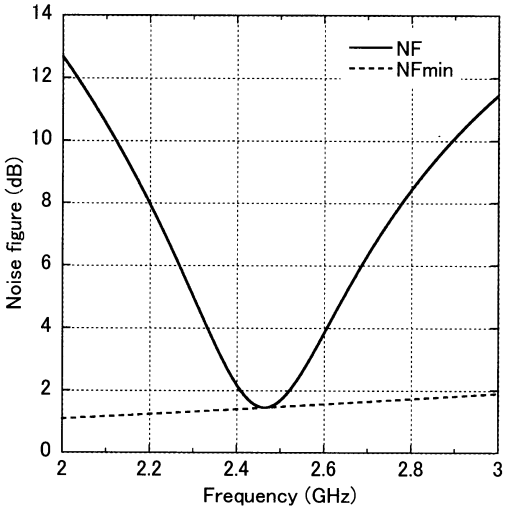

Fig. 14. Noise figure of the LNA with input and output matching circuit.

input and output sections are presented. Both input and output sections are almost matched to 50 Ω in the real part and 0 Ω in the imaginary part. By the present design method, a matching circuit using distributed transmission lines has become possible.

Usually, a small inductance is inserted between the source and the ground to make the real part of the impedance close to 50 Ω. However, the present design does not use a spiral inductor because elimination of the spiral inductor is extremely important for future enhancement of the operating frequency and functionality, as explained in Section 1. As a result, the calculation of the matching condition from the input impedance of the LNA designed in this paper indicates that an inductance of about 60 nH is needed at 2.45 GHz if the conventional spiral inductor (lumped element) is used. On the other hand, if the CPW (distributed circuit) proposed here is used, the area ratio can be reduced to about 1/2 and bandwidth design becomes possible. Hence, the chip size can be reduced dramatically. Further, if the spiral inductor is used in the present design rule, no other devices can be placed within a range of 50 μm due to magnetic field leakage from the inductor. On the other hand, the distributed transmission lines can be bent freely and are convenient for high degrees of integration.

6. Conclusions

By using a BPF formed with distributed transmission lines and inverter circuits, the filter and the matching circuit are integrated and realized on a CMOS chip. It is proposed in this way to design an RF-CMOS low noise amplifier and a power amplifier integrated with a filter. The analog circuit and the base band processor are placed on the same chip. The chip is presently under trial fabrication. The chip layout is shown in Fig. 16. In this figure, the matching circuit proposed in this paper is added only at the input of the LNA and the output of the PA. In general, lumped element devices such as spiral inductors cannot be used at higher frequencies due to self resonance. On the other hand, since the present matching circuit makes use of a resonant configuration, size reduction is possible as the frequency of operation is increased. Also, since filter circuit design is

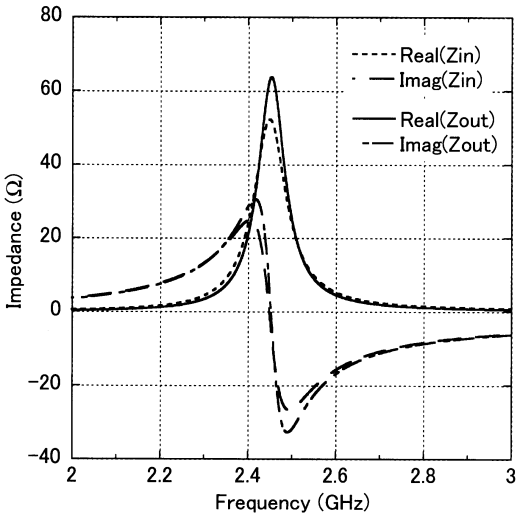

Fig. 15. Input and output impedance of the LNA with input and output matching circuit.

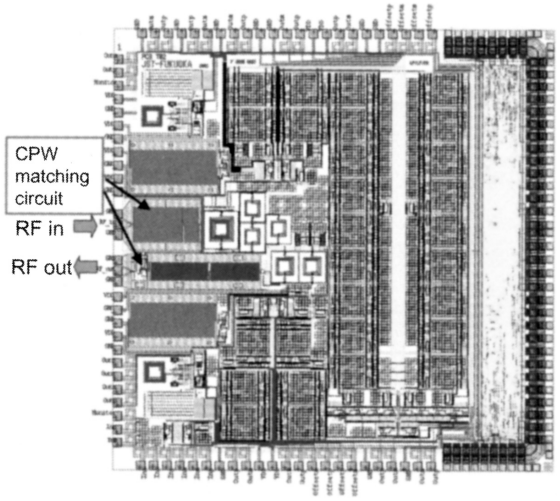

Fig. 16. Chip layout of RF-CMOS front-end (chip size: 5 mm × 5 mm).

possible in the present matching circuit, it is possible to carry out integrated design with a BPF by using multistage matching circuits.

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