Design of Coplanar Waveguide On-Chip Impedance-Matching Circuit for Wireless Receiver Front-End

H. Kanaya, R. K. Pokharel, F. Koga, Z. Arima, S. Kim, and K. Yoshida

Department of Electronics, Graduate School of Information Science and Electrical Engineering, Kyushu University, Fukuoka 812-8581, Japan

***Abstract* — Recently, spiral inductors have widely been used instead of resistors in the design of matching circuits to enhance the thermal noise performance of a wireless transceiver. However, such elements usually have low quality factor (Q) and may encounter the self-resonance in microwave-frequency band which permits its use in higher frequencies, and on the other hand, they occupy the large on-chip space. This paper presents a new design theory for the impedance-matching circuits for a single-chip SiGe BiCMOS receiver front-end for 2.4 GHz-band wireless LAN (IEEE 802.11b). The presented matching circuits are composed of conductor-backed coplanar waveguide (CPW) meanderline resonators and impedance (*K*) inverter. The prototype front-end receiver is fabricated and measured. A few of the measured results to verify the design theory are presented.**

***Index Terms* — CPW line, impedance-matching circuit, receiver front-end, transmission-line theory.**

I. Introduction

In the RF section of LSI chip, impedance-matching circuits are necessary for interconnecting each part such as low-noise amplifier (LNA), power amplifier (PA), duplexer, mixers, and so on, and lumped elements are usually used for the design of matching circuits. Among the lumped elements, spiral inductors are preferred in stead of resistors to enhance the thermal noise performance [1],[2]. However, they cannot be used at high frequency range because of the self-resonance and stray impedances. On the other hand, they also occupy large on-chip space.

Distributed elements made of transmission lines are particularly effective when their size becomes smaller, as the operating frequency increases. Distributed elements using transmission lines have already been implemented in GaAs based monolithic microwave integrated circuit (MMIC). However, it is necessary to fabricate the on-chip matching circuit based on distributed element, in order to operate the RF-CMOS or RF-BiCOMS LSI in the high frequency region.

Among various transmission lines, coplanar waveguide (CPW) line is easy to fabricate on the LSI chip because the signal line and ground plane exist on the same plane. In our previous studies [3],[4], some of the present authors proposed a design method of the CPW super-conducting impedance-matching circuit for interconnecting an antenna and duplexer.

In this paper, the design theory of the CPW impedance-matching circuits for single-chip SiGe BiCMOS LNA and down-conversion mixer (DCM) for wireless LAN (@2.4 GHz-band) is presented using a commercial electromagnetic (EM) and SPICE co-simulator (ADS2004A; Agilent Technologies), and verified by comparing the simulation with the results measured on a fabricated chip.

II. Design of LNA and DCM with On-Chip Impedance-Matching Circuit

Fig. 1 shows the block diagram of single-chip direct conversion transceiver which is composed of diode switch, LNA, PA, down-conversion mixer (DCM), and up-conversion mixer (UCM). In the figure, the LNA and PA are with input and output matching circuits. The design value of the input impedance and output impedance are 50Ω for general purpose.

Fig. 2 shows the schematics of the designed LNA and DCM. The DCM employs the double-balanced topology. The designed value of the Max gain of the LNA and noise figure (NF) is 17 dB and less than 3dB (@2.45 GHz) respectively. Similarly, the target conversion gain, NF, IF of the design mixer are 12 dB, less than 5 dB, and 15 MHz respectively. Each V_{CC} and V_{DD} of this process is 3.3V.

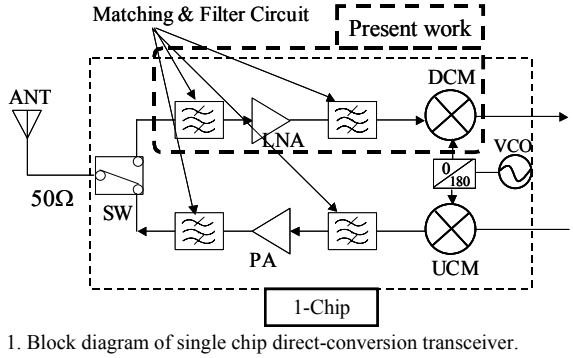
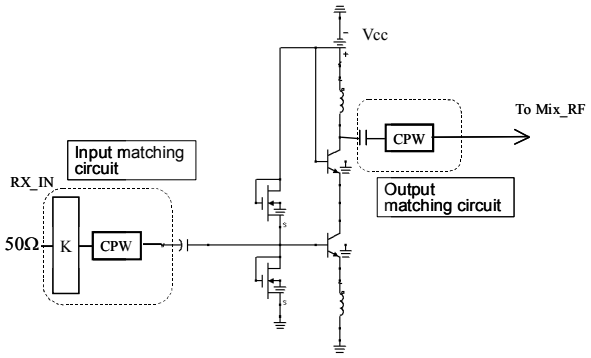
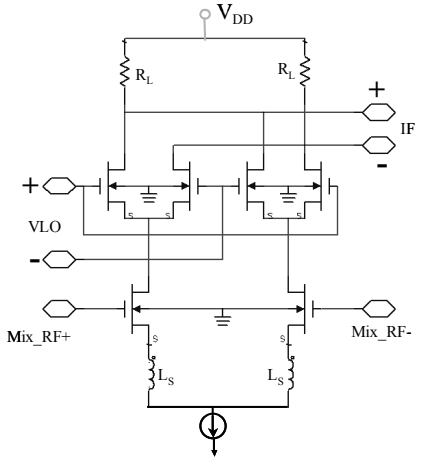


Fig. 1. Block diagram of single chip direct-conversion transceiver.



(a) Schematic of the designed LNA.



(b) Schematic of the designed DCM .

Fig. 2. Schematic of the designed LNA and DCM.

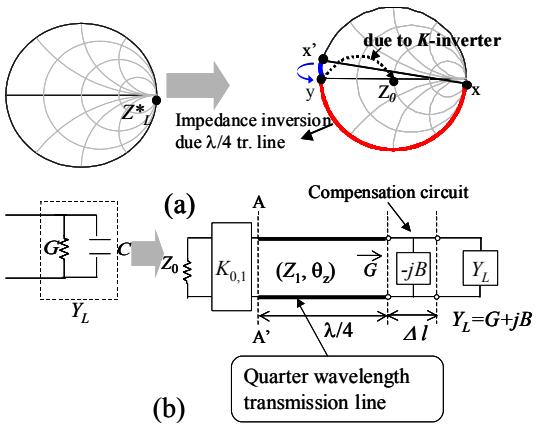


Fig. 3. Design and circuit model of impedance-matching circuit (a) Smith chart representation (b) circuit model using λ/4 CPW line and *K*-inverter.

In the present work, main focus is given on the design of the on-chip impedance-matching circuit for a receiver front-end using the transmission-line theory and its verification. The presented matching circuit is composed of the CPW meander lines and impedance inverter (*K*-inverter) or admittance inverter (*J*-inverter).

Fig. 3 shows the circuit model of the quarter wavelength (λ/4) matching circuits using *K*-inverter and its physical interpretation in Smith chart. Z_1, Y_1 and θ_x are the characteristic impedance, characteristic admittance and electrical length of the λ/4 line, respectively.

In Fig 3(a), Smith chart representation of the design theory of the matching circuit using λ/4 CPW line and *K*-inverter is illustrated. For example, Z^*_L is the conjugate of input impedance of LNA ($Z_L=1/Y_L$) and its position is shown by point x in the Smith chart.

The insertion of the λ/4-transmission line convertes the impedance to admittance, and its position is represented by x'. By using negative capacitance (-C), now its position will be shifted to new position, y and again due to *K*-inverter, the 50Ω-matching can be designed. A compensation circuit to achieve –C is realized by making the length of the transmission line slighly shorter than λ/4. In Fig. 3(b), an equivalent circuit representing the matching circuit is shown and its design parameters are computed by,

$$\begin{cases} \Delta\ell = -\dfrac{B}{\omega_0 C} \\ Z_1 = \dfrac{\pi}{4}\dfrac{w}{g_1 g_2 G} \\ K_{0,1} = \sqrt{w}\sqrt{\dfrac{Z_0 x_1}{g_0 g_1}}, \quad \left(x_1 = \dfrac{\pi}{4}Z_1\right) \end{cases}, \qquad (1)$$

where, C is the capacitance per unit length of the transmission line, and w and g_i are the normalized bandwidth and normalized filter element, respectively. $\Delta\ell$ is the line length in order to compensate the jB. The reactance (X_1) and the reactance slope parameter (x_1) are for the series resonance circuit [5]. One of the advantages of the presented method over lumped parameters is the independent selection of bandwidth, w in Eq. 1.

III. Fabricated Chip and Simulation Results

Fig 4 shows the microphotograph of a single-chip SiGe BiCMOS LNA and DCM for 2.4 GHz-band wireless LAN applications, and the proposed impedance-matching circuit interconnecting between them and at the input of the LNA. The chip is fabricated in TSMC0.35 μm one-poly three-metal BiCMOS technology.

The input and output pads have coplanar configurations so that characteristic impedances are 50Ω. Spiral inductors are used to apply DC power into the transistors and the LO ports of the mixer. There is a dummy metal in the center of the chip in order to suppress the RF noise.

There are also unused *K*-inverters and CPW lines which occupies more than 1/4th space in the fabricated chip (chip size: 2mm x 3.5 mm).

Fig. 5 shows the simulation results in the case of with and without the matching circuit between the LNA and DCM. The results confirm that the conversion gain of the mixer has been increased due to the matching circuit by the amount of voltage gain of the LNA in linear region. Please note that designed voltage gain of the LNA and the conversion gain of the DCM are 17 dB and 12 dB, respectively.

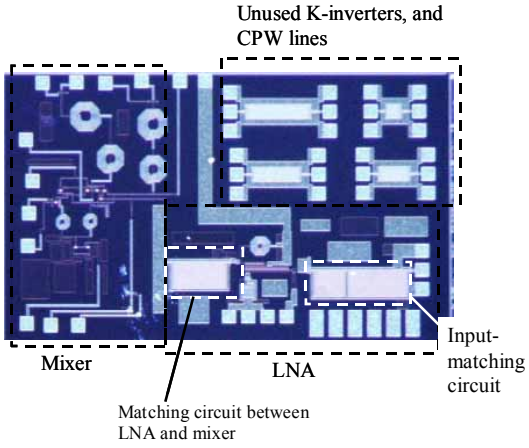


Fig. 4. Microphotograph of SiGe BiCMOS reciever front-end. (Chip size: 2mm x 3.5 mm)

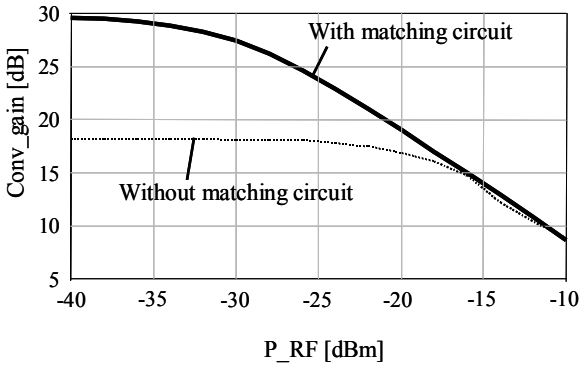


Fig. 5. Simulation results of the conversion gain of the mixer with and without the matching circuit between LNA and mixer.

IV. Measured Results

K-inverter is fabricated using shunt meander structure [5]. Fig. 6 shows microphotograph of *K*-inverter circuits which is designed using equation (1) and simulated by the EM simulator (Momentum, Agilent technologies). The design parameters of the matching circuit are f_0=2.45 GHz and w=100 MHz, which is based upon IEEE 802.11b. In order to avoid the loss in the Si-substrate, we covered the lowest metal (metal1) in all area of the CPW structure, namely conductor backed CPW. The conductance of the metal is 4.1x10^7 S/m. The signal width and the interval between the slots of the CPW transmission line are 5 μm and 15 μm, respectively. For size reduction, the λ/4 line was bended into meander structure.

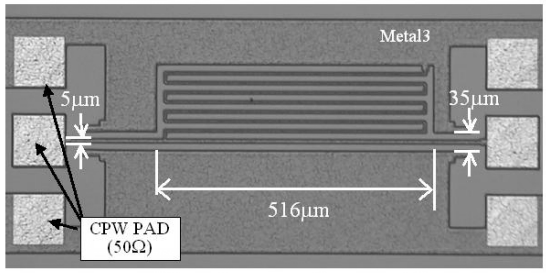


Fig. 6. Microphotograph of the *K*-inverter.(Taken out from another fabricated chip which is not shown in Fig. 4.).

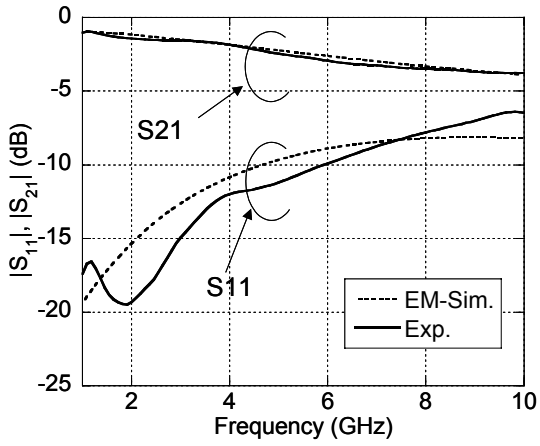


Fig. 7. Frequency responses of the CPW meanderline.

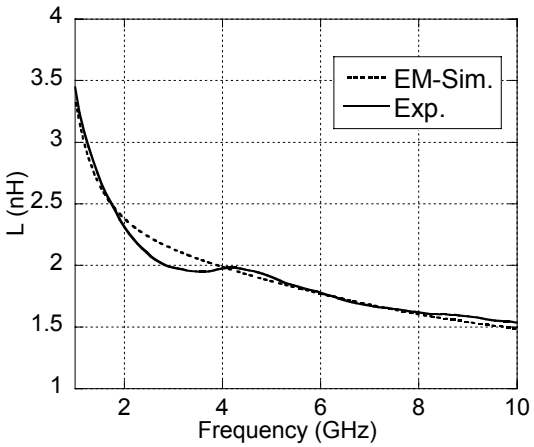


Fig. 8. Frequency dependence of the inductance (*L*) of the *K*-inverter

The input and output microwave characteristics are measured by using air coplanar probes (GSG 150; Cascade Microtech Inc.) and computed controlled vector network analyzer (HP-8722; HP). Fig. 7 shows the comparison of the frequency responses of the *K*-inverter. Insertion loss (S_{21}) of the EM-simulated result is almost in agreement with that of the experimental result. Fig. 8 show the frequency dependence of the inductance (L) of the *K*-inverter, calculated from the impedance matrix. Experimental value is almost in agreement with that of the EM-simulation result.

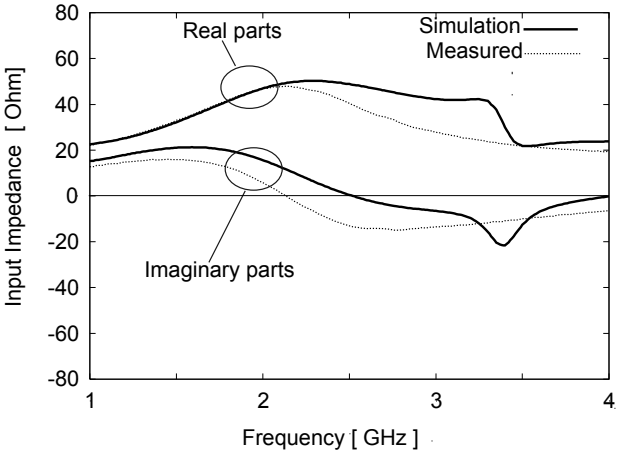


Fig. 9. Input impedance of the fabricated chip.

Fig. 9 shows the comparison of the measured and simulation results of the input impedance of the fabricated chip. In the figure, the measured results are in good agreement with the designed value. For example, the measured real part of the input impedance is about 47 Ω compared with 50 Ω of the designed value (@2.45 GHz). Similarly, the measured imaginary part is about –9 Ω compared to the +2 Ω of the designed value. This ensures that the validity of the presented method for the designing of the impedance-matching circuit using λ/4 CPW line and *K*-inverter.

V. Conclusion

Design methodology of impedance-matching circuit for a single chip SiGe BiCMOS receiver front-end which is composed of λ/4 CPW meander resonators and *K*-inverter is presented and verified by comparing the simulation results with measured results on a designed chip fabricated in TSMC0.35 μm SiGe BiCMOS technology. The CPW lines are realized by meander structures so that they can be fabricated inside a chip and their shape can be adjusted in order to exploit the vacant space on the substrate effectively. It takes less space than that of the spiral inductors. A rough comparison shows that the matching circuit designed by the proposed method takes 30% less space than that of the spiral inductors (@2.45GHz). If the operating frequency increases, this ratio becomes more effective. Another beauty of the transmission-line based matching circuit is the independent selection of the higher bandwidth, which is superior to the lumped element matching circuit.

When we design the receiver front-end such as LNA or mixer, the main target is not only to obtain maximum gain, but also maximum efficiency, minimum distortion, minimum noise figure, and so on, which depend on the specifications on demand. These optimum matching conditions are also realized by using the presented method instead of the lumped circuit element.

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