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Design and Verification of On-Chip Impedance-Matching Circuit Using Transmission-Line Theory for 2.4 GHz-Band Wireless Receiver Front-End

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SUMMARY Recently, spiral inductors have widely been used instead of resistors in the design of matching circuits to enhance the thermal noise performance of a wireless transceiver. However, such elements usually have low quality factor (Q) and may encounter the self-resonance in microwave-frequency band which permits its use in higher frequencies, and on the other hand, they occupy the large on-chip space. This paper presents a new design theory for the impedance-matching circuits for a single-chip SiGe BiCMOS receiver front-end for 2.4 GHz-band wireless LAN (IEEE 802.11b). The presented matching circuits are composed of conductor-backed coplanar waveguide (CPW) meander-line resonators and impedance (K) inverter. The prototype front-end receiver is designed, fabricated and tested. A few of the measured results to verify the design theory are presented.

key words: *CPW line, impedance-matching circuit, 2.4 GHz-band wireless LAN, $\lambda/4$ resonator, transmission-line theory*

1. Introduction

The explosive increase in the number of wireless communication equipments in the recent years enables the researchers to pay considerable efforts in the characteristics improvement of a wireless receiver front-end. In the mobile communication system, RF-CMOS LSI is a key technology in order to make size reduction and cost performance [1]–[3]. Although the performance of the CMOS chip has a limitation in the high frequency and high-speed applications, SiGe bipolar technology has a better frequency performance compared to CMOS at relatively low price compared to GaAs device [4], [5].

In the RF section of LSI chip, an impedance-matching circuit is necessary for interconnecting each part of the front-end such as low-noise amplifier (LNA), power amplifier (PA), duplexer, mixers, and so on, and lumped circuit elements are usually used. Among them, spiral inductors and MIM capacitors are preferred instead of resistors to enhance the thermal noise performance. However, they cannot be used at high frequency range because of the self-resonance and stray impedances, and on the other hand, they also occupy large on-chip space.

Distributed elements made of transmission lines are particularly effective when their size becomes smaller, as the frequency in use increases. Among the transmission lines, coplanar waveguide (CPW) line is easy to fabricate by the LSI technology compared to its counter part such as microstrip or strip lines because the signal line and ground plane exist on the same plane [6].

The applications of the distributed elements made of transmission lines were reported in the CMOS or BiCMOS RF-LSI chip [6]–[9]. The CPW lines was exploited as an inductor and used to design a conventional-type matching circuit for a LNA [6] in microwave-band frequency, and they were also used as an inductor in GaAs based monolithic microwave integrated circuit (MMIC) for millimeter-wave devices [7]. However, the application of CPW lines as an inductor takes larger on-chip space than a conventional spiral inductor [6]. Furthermore, CPW structures are implemented as phase controllers [8] and as open or short stubs for impedance-matching circuit for SiGe LSI chip in the Ka-band [9]. Some of the present authors have also implemented the CPW superconducting impedance-matching circuit for interconnecting an antenna and duplexer [10], [11].

In this paper, the design theory of the CPW impedance-matching circuit using the impedance (K) inverter and quarter-wavelength ($\lambda/4$) meanderline resonator for a single-chip SiGe BiCMOS receiver front-end for 2.4 GHz wireless LAN applications (IEEE 802.11b) is presented using a commercial electromagnetic (EM) and SPICE co-simulator (ADS2004A; Agilent Technologies). The receiver front-end consists of a LNA and down-conversion mixer (DCM) that uses double-balanced topology. The presented theory is verified by comparing the simulation with the results measured on a RF-LSI chip fabricated in TSMC 0.35 μm one-poly three-metal BiCMOS technology.

2. Design of LNA and DCM in 0.35 μm BiCMOS Process

2.1 Design of LNA and DCM with On-Chip Impedance-Matching Circuits

Figure 1 shows the block diagram of single chip transmitter (Tx) and receiver (Rx) amplifiers, which are composed of diode switch, LNA and PA with input and output matching circuits. The designed input and output impedances are 50 Ω for general purpose. We can combine the input and output

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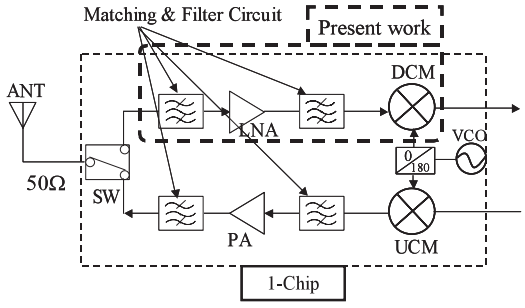
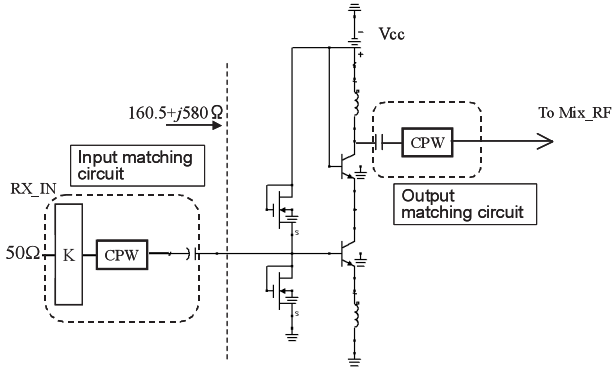
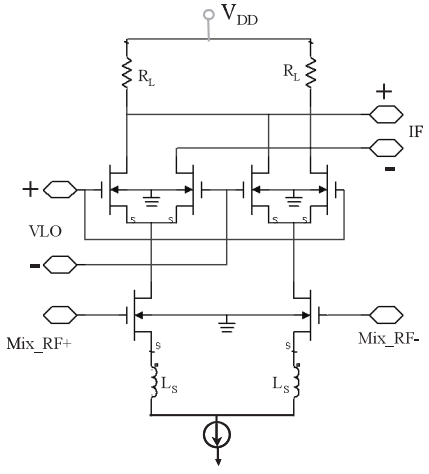


Fig. 1 Block diagram of single chip direct-conversion transceiver.



(a) Schematic of the designed LNA.



(b) Schematic of the designed DCM.

Fig. 2 Schematic of the designed LNA and DCM.

matching circuits and bandpass filter (BPF) together.

Figure 2 shows the schematics of the designed LNA and DCM. The DCM employs the double-balanced topology. A passive transformer is used as balun at the IF output of the mixer in the design. The designed value of the Max gain of the LNA and noise figure (NF) is 19 dB and less than 3 dB (@2.45 GHz) respectively. Similarly, the target conversion gain, NF, IF of the design mixer are 12 dB, less than 6 dB, and 15 MHz respectively. Each V_{CC} and V_{DD} of the 0.35 μm BiCMOS process is 3.3 V.

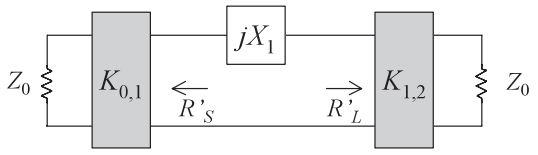


Fig. 3 Circuit model of one-pole BPF using K-inverter.

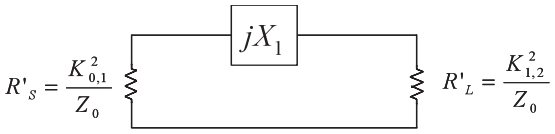


Fig. 4 Equivalent circuit model of the filter of Fig. 2 at the center part.

2.2 Design Theory of Matching Circuit

In the present work, main focus is given in the design and verification of the on-chip impedance-matching circuit for a receiver front-end using the transmission-line theory.

The present matching circuit is based on the theory of the n-pole Chebyshev bandpass filter (BPF) [12]. The BPF consists of distributed transmission lines and impedance inverters (K inverters, $K_{i,i+1}$). In usual wireless LAN cards, an off-chip dielectric filter is usually used as an external BPF and impedance matching is usually realized by off-chip bonding wires and sometimes on-chip spiral inductors. Realization of matching circuits using off-chip bonding wires is a difficult task because it needs a trial and error process. On the other hand, as also previously explained, conventional matching circuit using spiral inductors occupies large on-chip space and it also encounters self-resonance in microwave frequency band which permits its use beyond that frequency. Therefore, this paper employs a one-stage BPF as a matching circuit which can be realized inside a chip. The design formulae for a one-stage BPF using the impedance inverters (K inverters) shown in Fig. 3 are,

$$K_{0,1} = \sqrt{w}\sqrt{\frac{Z_0 x_1}{g_0 g_1}} \tag{1}$$

$$K_{1,2} = \sqrt{w}\sqrt{\frac{x_1 Z_0}{g_1 g_2}} \tag{2}$$

$$X_1 = x_1\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) \tag{3}$$

Here, Z_0 is the characteristic impedance, X_1 is the reactance in the series resonator with a reactance slope parameter x_1, w is the normalized bandwidth $(\omega_2 - \omega_1)/\omega_0$, and g_i is the filter parameter [12].

The equivalent circuit of the filter in Fig. 3 at the center part is shown in Fig. 4. Hence, the resistance ratio and the quality-factor (Q)value are given by,

$$\frac{R'_L}{R'_S} = \frac{Z_0}{K_{0,1}^2} Z_1^2 G_L = \frac{g_0}{g_2} \tag{4}$$

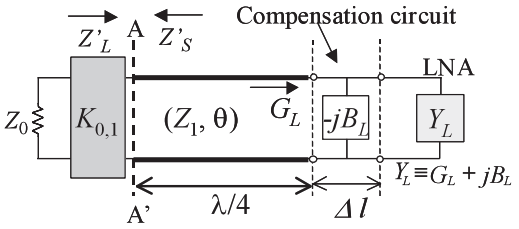


Fig. 5 Circuit model of the proposed matching circuit using $\lambda/4$ transmission line.

$$Q = \frac{x_1}{R'_S + R'_L} = \frac{Z_0}{K_{0,1}^2}\frac{x_1}{\left(1 + \dfrac{g_0}{g_2}\right)} = \frac{g_0 g_1 g_2}{w(g_0 + g_2)} \tag{5}$$

Next, we will explain a miniaturization design method for matching circuit employing a $\lambda/4$ transmission line. Figure 5 shows a new distributed impedance matching circuit proposed by the present authors using a K-inverter and a $\lambda/4$ transmission line. Here Y_L is the input admittance of the receiver front-end (say, of LNA) and is given by,

$$Y_L = \frac{1}{Z_L} \equiv G_L + jB_L \tag{6}$$

$$G_L = \frac{R_L}{R_L^2 + X_L^2}, \quad B_L = -\frac{X_L}{R_L^2 + X_L^2}$$

In the compensation circuit, Δl is determined by Eq. (7) in such a way that the susceptance B_L of the LNA is canceled out. Here, C (F/m) is the capacitance per unit length of the distributed transmission line.

$$\Delta l = -\frac{B_L}{\omega_0 C} = \frac{Z_L^2 X_L}{\omega_0 C(R_L^2 + X_L^2)} \tag{7}$$

Furthermore, in Fig. 5, if Z'_L is the impedance of the line looking from A-A′ of the K-inverter and Z'_s is impedance looking from $\lambda/4$ line towards K-inverter, then Z'_L and R'_S can be expressed in terms of the characteristics impedance Z_1 and the electrical length θ of the $\lambda/4$ transmission line as follows:

$$Z'_L = Z_1^2 G_L + jX_1 \equiv R'_L + jX'_L \tag{8}$$

where,

$$X_1 = -Z_1 \cot\theta \cong x_1\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right);$$

$x_1 = \frac{\omega_0}{2}\frac{\partial X}{\partial \omega}\Big|_{\omega=\omega_0} = \frac{\pi}{4}Z_1$: the reactance slope parameter of the series resonant circuit at $\omega = \omega_0$;

$$R'_L = Z_1^2 G_L;$$

$$R'_S = \frac{K_{0,1}^2}{Z_0}.$$

It is assumed in Eq. (8) that the input impedance of the LNA is sufficiently larger than Z_0 so that $|Y_L| \ll Y_0$. Hence, the equivalent circuit at A-A′ can be modified to that in Fig. 6.

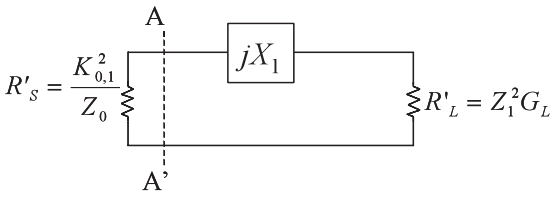


Fig. 6 Equivalent circuit model seen from A-A′.

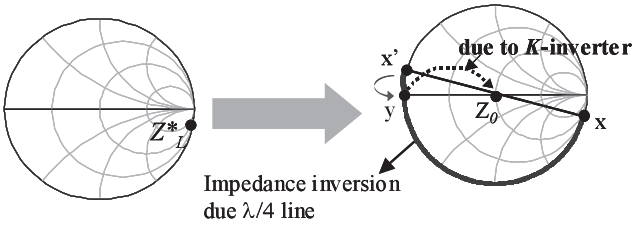


Fig. 7 Smith chart representation of the circuit model of the presented matching circuit using $\lambda/4$ line and K-inverter.

To make this structure identical to the 1-pole BPF, the resonant conditions can be found by substituting above values in Eqs. (4) and (5), respectively as,

$$\frac{R'_L}{R'_S} = \frac{Z_0}{K_{0,1}^2} Z_1^2 G_L = \frac{g_0}{g_2} \tag{9}$$

$$Q = \frac{x_1}{R'_S + R'_L} = \frac{Z_0}{K_{0,1}^2}\frac{x_1}{\left(1 + \dfrac{g_0}{g_2}\right)} = \frac{g_0 g_1 g_2}{w(g_0 + g_2)} \tag{10}$$

Here, please note that Eqs. (4), (5) and (9) and (10) are identical to each other, respectively. When these two equations are solved for $K_{0,1}$ and Z_1, we can eventually obtain the design formulae for the proposed matching circuit as follows:

$$Z_1 = \frac{\pi}{4}\frac{w}{g_1 g_2 G_L} \tag{11}$$

$$K_{0,1} = \sqrt{w}\sqrt{\frac{Z_0 x_1}{g_0 g_1}}, \quad \left(x_1 = \frac{\pi}{4}Z_1\right) \tag{12}$$

$$x_1 = \frac{\pi}{4}Z_1 \tag{13}$$

Therefore, impedance matching is possible with the characteristic impedance (Z_1) of the $\lambda/4$ transmission line and $K_{0,1}$ and on the other hand, it can realize BPF characteristics simultaneously. Also, it is found from Eq. (12) that the desired bandwidth can be obtained by varying w. If noise matching is used, the above can also be applied by letting $Y_L = Y^*_{opt}$ (Y_{opt} is the admittance minimizing the noise).

The physical interpretation of the design theory for presented matching circuit in Smith chart is illustrated in Fig. 7. For example, Z^*_L is the conjugate of input impedance of the receiver front-end ($Z_L = 1/Y_L$) (say of LNA) and its position is shown by point x in the Smith chart. The insertion of the $\lambda/4$-transmission line converts the high impedance to very low, and its position is represented by x' in the Smith chart. By using negative capacitance (−C), now its position will

be shifted to new position, y and again due to the K-inverter, the 50 Ω-matching can be designed. A compensation circuit to achieve −C is realized by making the length of the transmission line slightly shorter than $\lambda/4$.

In this paper, the input impedance of the receiver front-end is very high (160.5+j580 Ω), so matching circuit is designed using K-inverter. Due to this reason, the design theory using J-inverter is only introduced here, and detail study has been left for the future.

Furthermore, when the input impedance of the amplifier ($Z_L = R_L + jX_L$) is smaller than Z_0, the design parameters using the J-inverter can be derived in the similar way and are given by,

$$\begin{cases} \Delta\ell = -\frac{X_L}{\omega_0 L} \\ Y_1 = \frac{1}{Z_1} = \frac{\pi}{4}\frac{w}{g_1 g_2 R_L} \\ J_{0,1} = \sqrt{w}\sqrt{\frac{Y_0 b_1}{g_0 g_1}}, \quad \left(b_1 = \frac{\pi}{4}Y_1\right) \end{cases}, \tag{14}$$

where, L is the inductance per unit length of the transmission line, and w and g_i are the normalized bandwidth and normalized filter element, respectively. $\Delta\ell$ is the line length in order to compensate the jX_L. The susceptance (Y_1) and the reactance slope parameter (b_1) are for the shunt resonant circuit [12].

3. Design of Passive Elements and Accuracy of Co-Simulation of SPICE-Type and EM-Simulator

In this paper, we use one of the most widely used tools known as Advanced Design System (ADS2004A, Agilent Technologies) in designing of CMOS or BiCMOS circuits and Momentum (Agilent Technologies) for electromagnetic characterization of passive elements. The ADS is a SPICE-type circuit simulator and Momentum is an electromagnetic simulator based on the method of moments. The Co-Simulation option uses both circuit-type simulation and EM simulation simultaneously to provide an interesting option to design and simulate CMOS or BiCMOS circuits with EM characterization of passive devices in LSI chip.

In order to evaluate the accuracy of EM simulator, we fabricate the on-chip spiral inductor, and compare the SPICE models and experimental results with EM simulation results in this Section.

3.1 Design of Spiral Inductor

We use the 0.35 μm BiCMOS process in TSMC, which has 1 Poly and 3 metal structures and the thickness of the top metal is 3.1 μm as shown in Fig. 8. The conductance of the metal and ε_r of the SiO_2 are 4.1×10^7 S/m and 4.1, respectively. Figure 9 shows the layout and chip photograph of the EM simulation of the spiral inductor with guard ring and CPW pads (Total IND), and open dummy. The open dummy is necessary to estimate the value of the inductor to be discussed latter. Please note that a small stub at the center CPW pad (dummy pad of right side) in Fig. 9(a) is to compensate

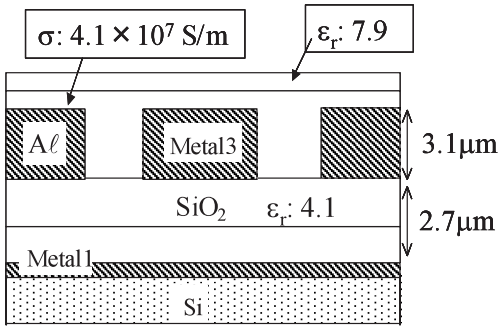


Fig. 8 Sectional view of the used 0.35 μm BiCMOS process.

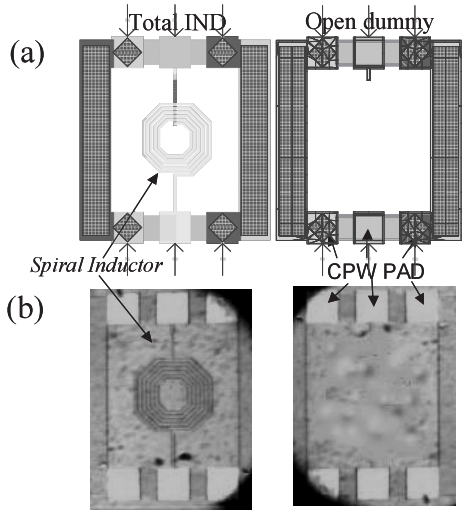


Fig. 9 EM simulation layouts (a) and photographs (b) of the spiral inductor and open dummy.

the interconnect between metal 2 terminal of the spiral inductor and the pad. The line width and spacing of the spiral inductor is 10 μm each other. The CPW pad is 100 μm square and designed in such as way that its characteristic impedance is to be 50 Ω. The microwave characteristics are measured by using air coplanar probe (Cascade Microtech, GSG150) and vector network analyzer (HP, HP8722C).

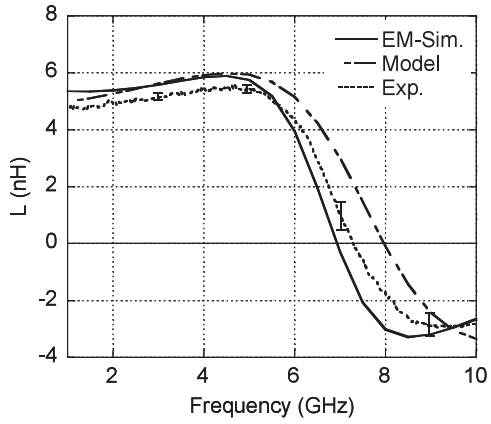
The measured data must be de-embedded in order to remove the parasitic effects of interconnects, pads and contacts surrounding the device [13]. At first, we measure S-parameters of total IND and open dummy. Next, S-parameters are transformed into Y-parameter, and removed the parallel circuits and parasitic elements as follows

$$[Y]_{\text{spiral}} = [Y]_{\text{total}} - [Y]_{\text{dummy}} \tag{15}$$

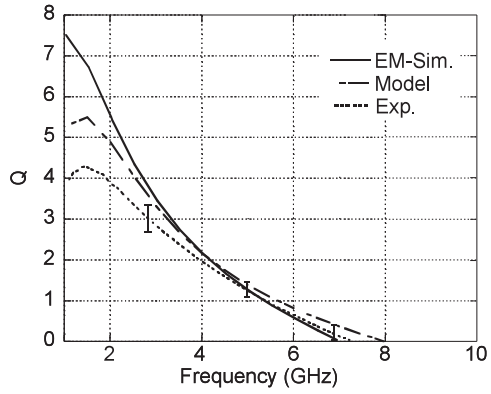
Finally, $[Y]_{\text{spiral}}$ is converted to Z-parameters, and inductances (L) and quality factors (Q) are calculated as follows

$$\begin{cases} L = \text{Im}(Z_{in})/(2\pi f) \\ Q = \text{Im}(Z_{in})/\text{Re}(Z_{in} - 50) \end{cases}. \tag{16}$$

Figure 10 shows the frequency dependences of inductance and Q-value of the T=5.5 spiral inductor, where "T" is



(a) L of smaller spiral inductor (T=5.5)



(b) Q-value of smaller spiral inductor (T=5.5)

Fig. 10 Frequency dependence of L and Q-value of the spiral inductors.

the turn number of the spiral inductor. In the figure, "Model" means that of the SPICE models. The EM simulation results are consistent with the experimental results than that of the SPICE models. This verifies the importance of co-simulation during LSI design using the SPICE tools in order to model the spiral inductors. Therefore, co-simulation technique is used to model the spiral inductors in BiCMOS circuit throughout this paper. As evidenced in Fig. 10, the model spiral inductor (T=5.5) has a self-resonance around 5.5 GHz, and does not work as an inductor beyond that frequency.

3.2 Design of Transmission Lines

The components of a CPW matching circuit are designed and simulated by the EM simulator (Momentum, Agilent technologies) in this section. Please note that the presented matching circuit is composed of K-inverter and $\lambda/4$ resonator, both of them are realized on CPW meander structures. The design parameters of the matching circuit are f_0=2.45 GHz and w=4% (100 MHz/2.45 GHz), which is based on the IEEE 802.11b Standards. In order to avoid the loss in the Si substrate, we covered the lowest metal (metal1) in all area of the CPW structure, namely conductor backed CPW. Figure 11 shows the chip photo of the conductor backed CPW resonator with CPW PAD. The signal

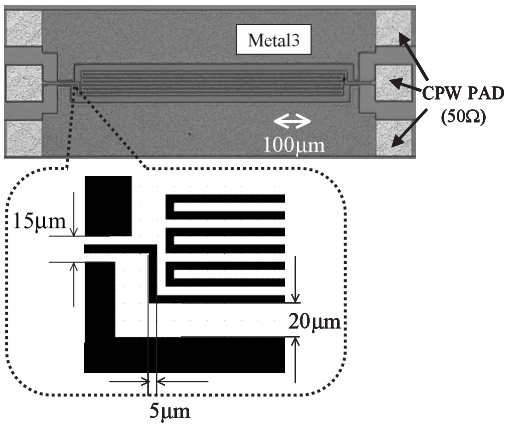


Fig. 11 Chip photo of the conductor backed CPW transmission line. (line length =13 mm)

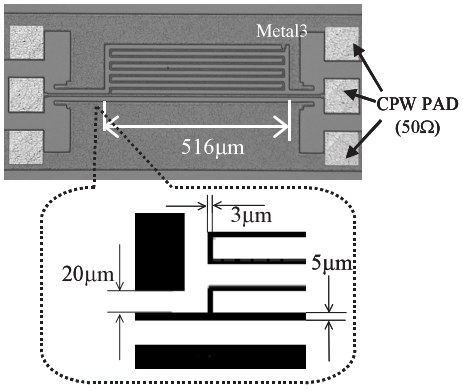


Fig. 12 Chip photo of meander inductor of the K-inverter.

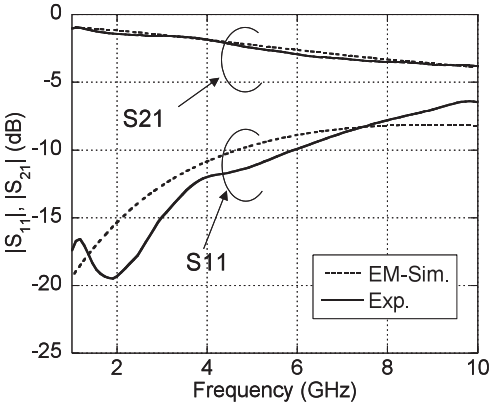


Fig. 13 Frequency responses of the conductor-backed CPW meander line.

width and the interval between the slots of the CPW transmission line are 5 μm and 15 μm, respectively so that its characteristic impedance is to be 50 Ω. For size reduction, the $\lambda/4$ line (line length = 13 mm) is bended into meander structure. Similarly, Fig. 12 shows the chip photo of the K-inverter with CPW PAD.

Figure 13 shows the comparison of the frequency responses of $\lambda/4$ conductor-backed CPW line which is con-

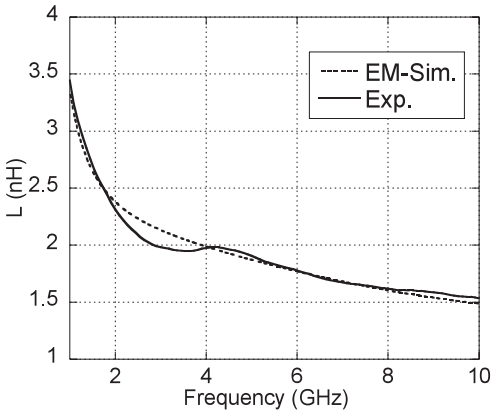


Fig. 14 Frequency dependence of the inductance (L) of the K inverter.

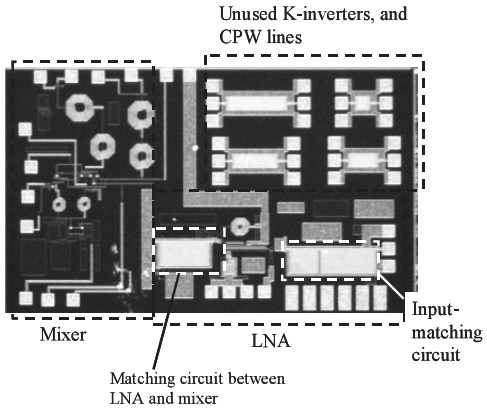


Fig. 15 Microphotograph of SiGe BiCMOS receiver front-end. (Chip size: 2 mm × 3.5 mm)

structed on meander structure. Insertion loss (S_{21}) of the EM-simulated result is almost in agreement with that of the experimental result. Figure 14 shows the frequency dependence of the inductance (L) of the K-inverter, calculated from the impedance matrix. Experimental value is almost in agreement with that of the EM-simulation result. This ensures the validity of EM simulation in designing the distributed circuits using CPW transmission lines.

4. Fabricated Chip and Measured Results

Figure 15 shows the microphotograph of a single-chip SiGe BiCMOS LNA and DCM for 2.4 GHz-band wireless LAN applications, and the proposed impedance-matching circuit interconnecting between them and at the input of the LNA. The chip is fabricated in TSMC0.35 μm one-poly three-metal BiCMOS technology.

The input and output pads have coplanar configurations so that characteristic impedances are 50 Ω. Spiral inductors are used to apply DC power into the transistors and the LO (Local) ports of the mixer. There is a dummy metal in the center of the chip in order to suppress the RF noise. There are also unused K-inverters and CPW lines which occupies more than 1/4th space in the fabricated chip (chip size: 2 mm × 3.5 mm).

Figure 16 shows the simulation results in the case of with and without the matching circuit between the LNA and DCM. The results confirm that the conversion gain of the mixer has been increased due to the matching circuit by the amount of voltage gain of the LNA in linear region. Please note that designed voltage gain of the LNA and the conversion gain of the DCM are 19 dB and 12 dB, respectively. About 1.5 dB-loss can be attributed to the loss in CPW lines at 2.45 GHz as noted from Fig. 13.

Figure 17 shows the comparison of the measured and simulation results of the input impedance of the fabricated chip. In the figure, the measured results are in good agreement with the designed value. For example, the measured real part of the input impedance is about 47 Ω compared with 50 Ω of the designed value (@2.45 GHz). Similarly, the measured imaginary part is about −9 Ω compared to the

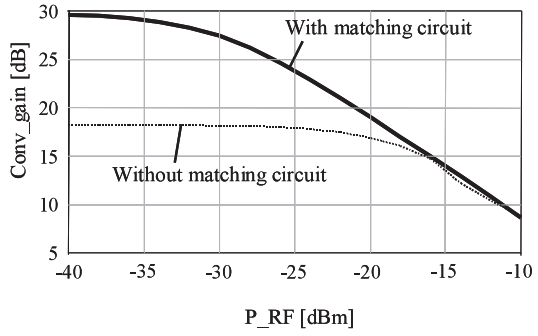


Fig. 16 Simulation results of the conversion gain of the mixer with and without the matching circuit between LNA and mixer. (P_RF represents the input power at RF port and Conv_gain is the conversion gain of the mixer).

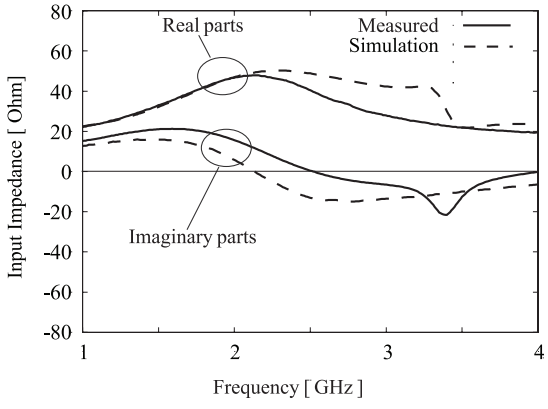
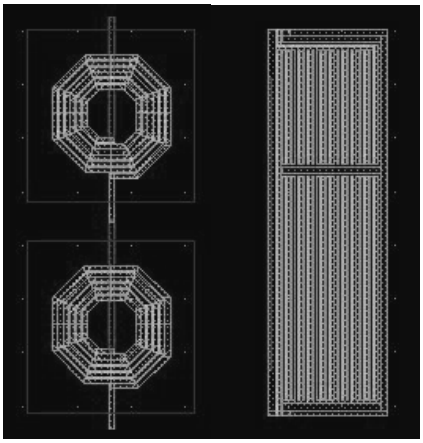


Fig. 17 Input impedance of the fabricated chip.

+2 Ω of the designed value. This ensures that the validity of the presented method in designing the on-chip impedance-matching circuit using $\lambda/4$ CPW line and K-inverter.

Figure 18 shows the comparison of on-chip area occupied by the matching circuit designed using spiral inductors based on the conventional method and the presented theory, respectively. In the comparison, the size of MIM capacitor which is a part of the matching circuit and also work as a D.C. block capacitor, are approximately the same,



(a) (b)

Fig. 18 Comparison of on-chip area occupied by matching circuit (a) Layout of spiral inductors (total=13.8 nH) required for matching designed by conventional theory. (size=370 μm × 790 μm) (b) Layout of $\lambda/4$ CPW line and K-inverter for matching designed by the presented theory. (size=240 μm × 780 μm)

and therefore ignored in the size comparison. In Fig. 18(a), the layout of the spiral inductors required for the matching of the designed receiver front-end is shown whose size is 370 μm × 790 μm in the TSMC 0.35 μm BiCMOS foundry. In the figure, two spiral inductors were used to realize the required L and there should be at least 4 μm space left between the inductor's active areas according to the foundry's design rules. For the same purpose, the required space taken by the matching circuit by the presented theory is shown in Fig. 18(b) where the size is only 240 μm × 780 μm, thus saving the valuable chip area about by 30%. If the operating frequency increases, this ratio becomes more effective. However, comparison of the presented method with those using by a combination of a short transmission line for phase shift and a quarter-wavelength transformer has not been investigated yet and will be taken as one of the priority works in the near future.

5. Conclusions

Design methodology of impedance-matching circuit for a single chip SiGe BiCMOS receiver front-end which is composed of $\lambda/4$ CPW meander resonators and K-inverter is presented and verified by comparing the simulation results with measured results on a designed chip fabricated in TSMC 0.35 μm SiGe BiCMOS technology. The CPW lines are realized by meander structures so that they can be fabricated inside a chip and their shape can be adjusted in order to exploit the vacant space on the substrate effectively. It takes less space than that of the spiral inductors. A rough comparison shows that the matching circuit designed by the proposed method takes about 30% less space than that of the spiral inductors (@2.45 GHz). If the operating frequency increases, this ratio becomes more effective. Another beauty of the transmission-line based matching circuit is the freedom of selection of the higher bandwidth, which is superior to the lumped element matching circuit.

The accuracy of co-simulation technology in designing the passive circuits in LSI chip is also discussed by comparing the simulation results with the experiment, and it shows that EM simulation is superior to the SPICE models of the spiral inductor.

When we design the receiver front-end such as LNA or mixer, the main target is not only to obtain maximum gain, but also maximum efficiency, minimum distortion, minimum noise figure, and so on, which depend on the specifications on demand. These optimum matching conditions are also realized by using the presented method instead of the lumped circuit element.

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