Development of a HTS Slot Antenna With Multi-Bandpass Filters

H. Kanaya, *Member, IEEE*, T. Hashiguchi, R. K. Pokharel, *Member, IEEE*, and K. Yoshida, *Member, IEEE*

***Abstract*—We developed a single-chip receiver antenna combined with coplanar waveguide (CPW) impedance matching circuits and multi-bandpass filters (multiplex receiver). Firstly, we designed a HTS slot antenna with 10.5 GHz center frequency. Next, in order to compensate the reactance of the antenna at different center frequencies of the BPFs, we attached the reactance compensation transmission lines behind the Y-junctions. Finally, we design the channel #1 BPF and channel #2 BPF matched to the input impedance of the antenna and reactance compensation line. The channel #1 BPF has center $\mathrm{frequency} = 10.3\ \mathrm{GHz}$ and channel #2 BPF has center $\mathrm{frequency} = 10.7\ \mathrm{GHz}$. The prototype YBCO 2-channel BPFs was fabricated and verified the design theory.**

***Index Terms*—Coplanar waveguide, impedance matching circuit, multiplexer, slot antenna.**

I. Introduction

In RECENT years, many RF passive devices made of high T_c superconducting (HTS) thin films, such as bandpass filter (BPF), have been studied, which have extremely low surface impedance at microwave frequencies.

It is widely known, however, that in order to realize HTS antenna we must simultaneously realize an impedance matching circuit, which compensates the narrow bandwidth (or high quality factor) peculiar to the superconducting small antenna [1]. Moreover, it will be necessary to combine some RF front-end devices for multi channel applications.

So, we will fabricate the HTS single-chip receiver antenna combined with broadband impedance matching circuits and duplexer or multiplexer with BPFs.

There are many reports of surface acoustic wave (SAW) duplexers, and SAW duplexers are already used commercially [2]. However, because SAW duplexer has thee dimensional structure, it is difficult to realize single chip RF front-end. On the other hand, duplexer composed of planar type passive devices such as coplanar waveguide (CPW) bandpass filter (BPF) is easy to fabricate on the single chip, because the signal line and ground plane exist only on the same side, and also easy to realize desired characteristic impedance. There are some reports about planar type duplexer which has 50 Ω input and output ports [3].

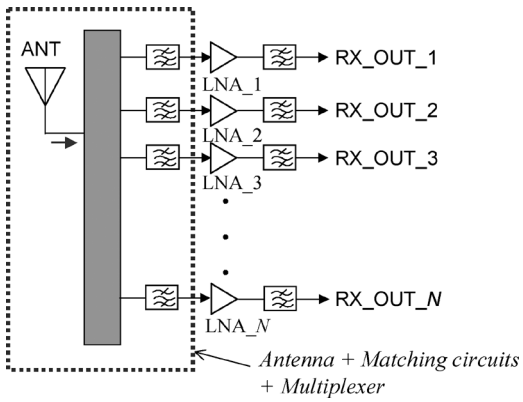

Fig. 1. Block diagram of a multi-channel receiver with slot antenna.

Additionally, in the RF section, impedance matching circuit is necessary for interconnecting antenna, duplexer low noise amplifier (LNA) and power amplifier (PA). It is particularly effective to fabricate the matching circuit by using distributed elements made of transmission lines because their size becomes smaller, as the frequency is higher.

In our previous papers [4], [5], we proposed a design method of the broadband impedance matching circuit for interconnecting the single-chip devices such as small antenna, CMOS LNA and PA.

In this paper, we designed the planar antenna combined with coplanar waveguide (CPW) impedance matching circuits and duplexer for HTS single chip multi-channel receiver. Fig. 1 shows the block diagram of a multi-channel receiver with antenna.

II. Design of Antenna Combined With CPW Impedance Matching Circuits and Duplexer

A. Design of a Slot Antenna

We adopted the slot dipole antenna as shown in Fig. 2(a), which is fed by CPW transmission line. The size of the antenna section is 12 mm × 8 mm. The widths of the signal line and between the ground conductors in the CPW feed line are 35 μm and 66 μm, respectively, and ε_r of the substrate is 9.6, which has 50 Ω characteristic impedance. We assumed the loss-less conductor is placed on the MgO substrate with thickness on 500μm. Fig. 2(b) shows the circuit model of the antenna section. Our slot antenna has a series resonance. Fig. 3 shows the S parameter of the slot antenna. The geometry of the slot antenna was adjusted

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The authors are with Department of Electronics, Graduate School of Information Science and Electrical Engineering, Kyushu University, 744 Motooka, Nishi-ku, Fukuoka 819-0395, Japan (e-mail: kanaya@ed.kyushu-u.ac.jp).

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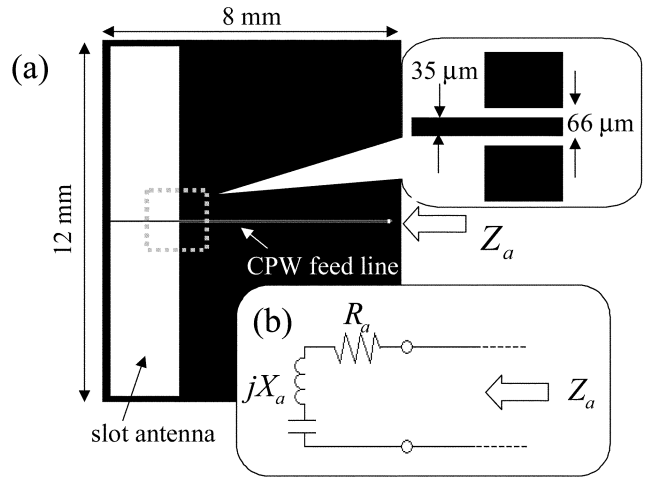

Fig. 2. EM simulation layout of slot antenna 2(a) and circuit model of antenna section 2(b).

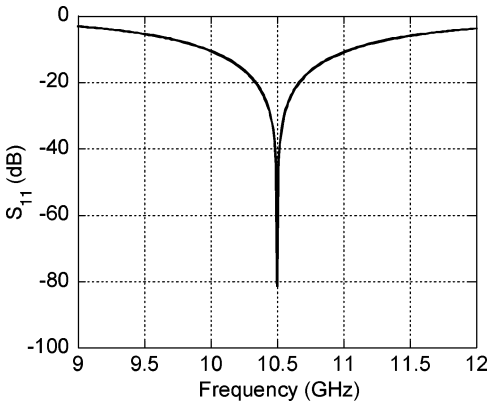

Fig. 3. EM simulation result of the return loss of the slot antenna.

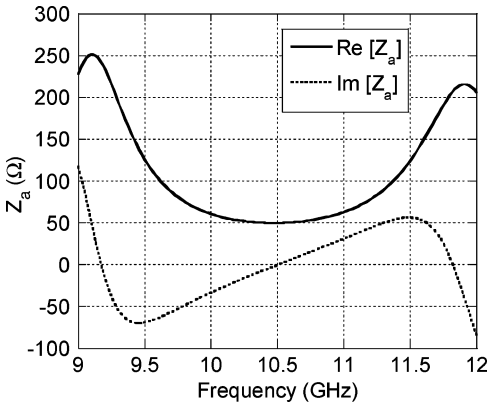

Fig. 4. Frequency dependence of the antenna impedance.

so that the center frequency is 10.5 GHz. Fig. 4 shows the frequency dependence of the antenna impedance $Z_{\rm a} = R_{\rm a} + jX_{\rm a}$, which is calculated by using electro magnetic (EM) simulator (ADS, Agilent technologies).

For multi-channel receiver, the center frequency of a channel #1 is assumed to be 10.3 GHz and a channel #2 is assumed to

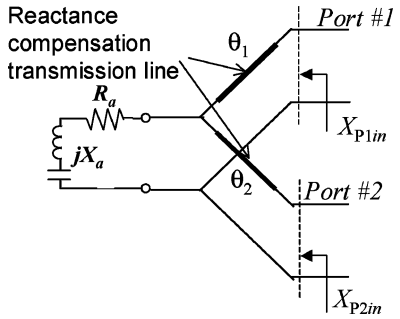

Fig. 5. Circuit model of the reactance compensation transmission line.

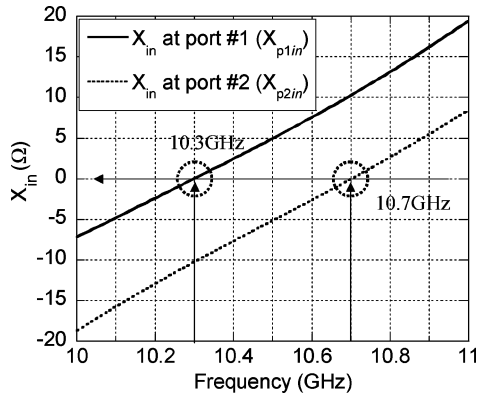

Fig. 6. Frequency dependence of $X_{\rm P1}{}_{in}$ and $X_{\rm P2}{}_{in}$.

be 10.7 GHz, respectively. In order to separate the RF signal of channel #1 (port #1) and #2 (port #2), Y-junction is attached on the CPW feed line.

As shown in Fig. 4, $Z_{\rm a} = R_a + jX_a$ at $f_{\rm P1} = 10.3$ GHz and $f_{\rm P2} = 10.7$ GHz are $52 - j12\ \Omega$ and $52 + j12\ \Omega$, respectively, where, "P1" and "P2" is the port number. In order to compensate the imaginary part, CPW transmission lines (electrical length $= \theta_1$ and θ_2) are attached on the Y-junction, as shown in Fig. 5. Fig. 6 shows the frequency dependence of $X_{\rm P1}{}_{in}$ and $X_{\rm P2}{}_{in}$ of $\theta_1 = 3.227$ rad, and $\theta_2 = 3.058$ rad. As shown in Fig. 6, the reactance is zero at 10.3 GHz and 10.7 GHz, respectively.

The real part of the input impedances ($R_{\rm P1}{}_{in}$, $R_{\rm P2}{}_{in}$) is inverted into 50 Ω by using admittance inverter as shown in the next subsection.

B. Design of Matching Circuit and Duplexer

Fig. 7 shows the circuit model of the antenna with matching circuit and duplexer. The n-pole Chebyshev BPFs with matching circuit are attached on the reactance compensation lines, which have different resonant frequency, namely, $f_{\rm P1} = 10.3$ GHz and $f_{\rm P2} = 10.7$ GHz, respectively.

In the figure, $J'_{{\rm P1}(n,n+1)}$, $J'_{{\rm P1}(n-1,n)}$, $J'_{{\rm P2}(n,n+1)}$, $J'_{{\rm P2}(n-1,n)}$, $J_{{\rm P1}(i,i+1)}$ and $J_{{\rm P2}(i,i+1)}$ are admittance inverters (J inverters) composed of the matching circuit in the BPF. $b_{{\rm P1},n}$, $b_{{\rm P2},n}$, $b'_{{\rm P1},n}$ and $b'_{{\rm P2},n}$ are susceptance slope parameters of the susceptance ($B_{{\rm P1},n}$, $B_{{\rm P2},n}$, $B'_{{\rm P1},n}$ and $B'_{{\rm P2},n}$) of the parallel resonance.

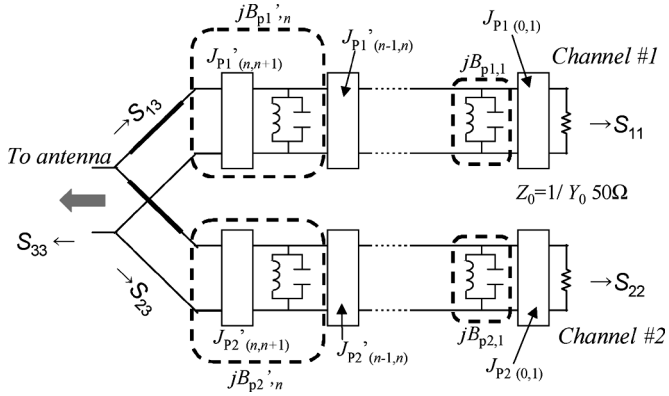

Fig. 7. Circuit model of the antenna with n-pole matching circuit and duplexer. S_{ij} is S-parameter.

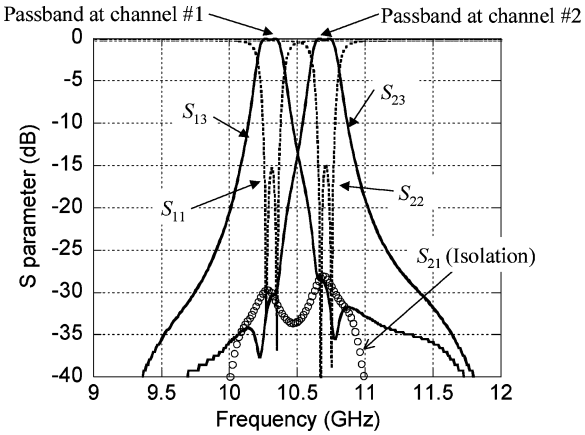

Fig. 8. Frequency responses of the circuit model of the $n = 2$ duplexer.

J inverters of the antenna section are described in our previous paper [6], and are written for port #1 by,

$$J'_{P1(n,n+1)} = \sqrt{w_{P1}}\sqrt{\frac{b'_{P1,n}}{g_n R_{P1in}}}, \quad (1)$$

$$J'_{P1(n-1,n)} = w_{P1}\sqrt{\frac{b_{P1,(n-1)}b'_{P1,n}}{g_{n-1}g_n}}, \quad (2)$$

$$J_{P1(i,i+1)} = w_{P1}\sqrt{\frac{b_{P1,i}b_{P1,(i+1)}}{g_i g_{i+1}}}, \quad (i=1,2,\cdots n-2) \quad (3)$$

$$J_{P1(0,1)} = \sqrt{w_{P1}}\sqrt{\frac{Y_0 b_{P1,1}}{g_0 g_1}}, \quad (4)$$

$$b'_{P1,n} = \frac{b_{P1,n}}{1 - \frac{w_{P1}x_{P1in}}{R_{P1in}g_n}} \quad (5)$$

Where, w_{P1} is the fractional bandwidth and g_n is the filter parameters of the Chebyshev type $\lambda/2$ resonator BPF [7]. $x_{\mathrm{P1}in}$ is the reactance slope parameter of the reactance $X_{\mathrm{P1}in}$

We can obtain the design parameters for port #2 in the replacement of subscript "$P1$" with "$P2$".

III. Simulation Results of Single-Chip Antenna Combined With CPW Duplexer

Fig. 8 shows the frequency responses of the circuit model of the two-pole $(n = 2)$ duplexer. The -16 dB bandwidth

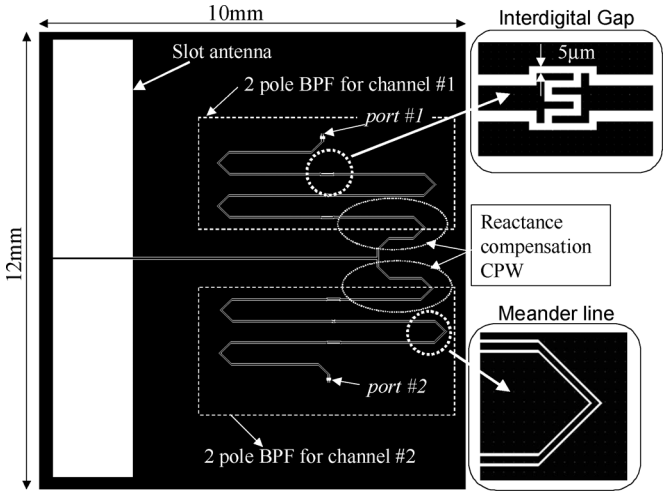

Fig. 9. Layout of the slot antenna with $n = 2$ duplexer.

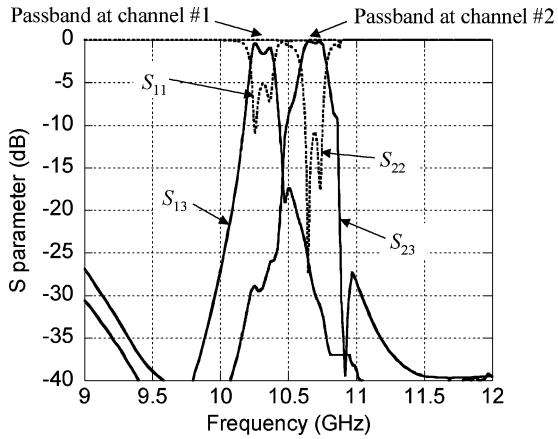

Fig. 10. EM simulation results of the duplexer.

(design ripple $= 0.1$ dB) and isolation between the ports of the duplexer are 100 MHz and -28 dB, respectively.

Fig. 9 shows the layout of the slot antenna with $n = 2$ duplexer for EM simulation. J inverters are realized by the interdigital gaps. The line and space width of the interdigital gap are 5 μm, respectively. For size reduction, the $\lambda/2$ resonator composed of CPW transmission line was bent into meander structure. (See Fig. 9). The widths of the signal line and between the ground conductors in the CPW duplexer are the same configurations in the antenna section. [See Fig. 2(a)]. The total size of the single-chip antenna with impedance matching circuit and duplexer is 10 mm $\times$ 12 mm. Fig. 10 shows the EM simulation results of the duplexer. The EM simulation results of the both center frequencies and bandwidths are similar to those the circuit model. However, because of the unexpected electromagnetic couplings between the resonators, off-band responses and design ripple are different from those of the circuit model.

IV. Experimental Results and Discussion of Prototype YBCO Duplexer

Fig. 11 shows the layout and photograph of the prototype YBCO CPW duplexer. In order to confirm our design theory, the 50 Ω port is attached instead of the slot antenna. (See port

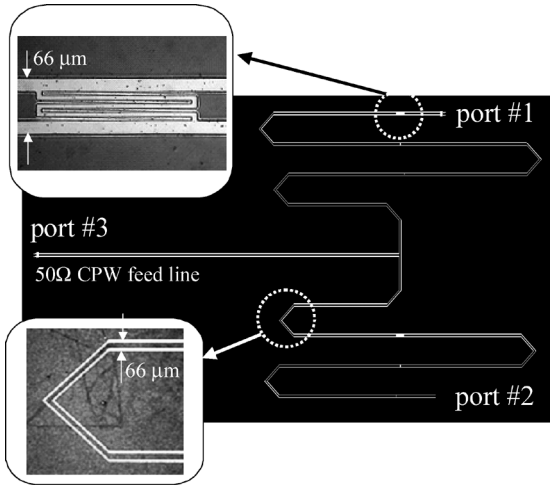

Fig. 11. Layout and photograph of the prototype YBCO CPW duplexer.

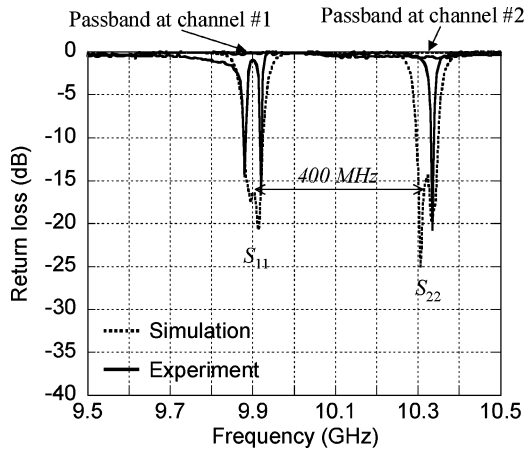

Fig. 12. Frequency responses of the YBCO CPW duplexer at 20 K.

#3 in Fig. 11). In the figure, the meander structure and interdigital gap are also printed. YBCO film used in this experiment was prepared on MgO single crystal, which has $\varepsilon_{\mathrm{r}} = 9.6$ and $\mathrm{thickness} = 500\ \mu\mathrm{m}$. The YBCO film thickness is 0.8 μm. The duplexer was fabricated by the wet etching process. In the figure, we can see the over etching portion in the interdigital gap. This duplexer was placed in a vacuum chamber with refrigerator cooling system. A vector network analyzer (HP8722C; HP) measured the S parameters though the air coplanar probes (GSG-150; Cascade Microtech).

Fig. 12 shows the frequency responses of the YBCO CPW duplexer at 20 K. These characteristics include the residual loss due to the contact between the YBCO film and air coplanar metal probes. In Fig. 12, the broken line shows the S parameters of the loss less circuit model. The center frequencies are shifted to the lower frequency because of the kinetic inductance of the YBCO, the effect of errors in the dielectric constant and thickness of the substrate, so that simulation data is shifted to the lower frequency. The shifted channel center frequencies and bandwidth are similar to that of the circuit model. Because of the contact loss and over etching, design ripple is not in full agreement with the simulation result. However, we can verify our new design theory by cryogenic experiment. In order to reduce the over etching portion, it will be necessary to fabricate the YBCO duplexer by the dry etching process like an electron beam etching.

V. Conclusion

For realizing the HTS receiver, we developed the singe-chip receiver antenna combined with Y-junction, reactance compensation CPW line, impedance matching circuits and duplexer. We designed the 2-pole BPFs which have center $\mathrm{frequency} = 10.3$ GHz and 10.7 GHz, respectively. Finally, a prototype YBCO duplexer was fabricated and tested at cryogenic temperature.

By using the CPW BPF with attenuation poles, which was introduced in our previous paper [8], [9], we can realize the highly selective duplexer.

Moreover, we can design the HTS multiplexer by adding the reactance compensation CPWs, matching circuit with BPFs.

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