DEVELEOPMENT OF A SINGLE-CHIP RF FRONT-END LSI FOR WIRELESS LAN WITH TRANSMISSION LINE BASED MATCHING CIRCUITS

R. K. Pokharel, A. Imada, H. Kanaya, and K. Yoshida
Department of Electronics, Kyushu University
744 Motooka, Nishi-ku Fukuoka 819-0395, Japan
Email: pokharel@ed.kyushu-u.ac.jp

Abstract: In Direct Conversion Receiver (DCR) architecture, the design of mixer is one of the most important steps for a high-performance DCR because it involves the issues of flicker (1/*f*) noise and conversion gain simultaneously. So, minimizing 1/*f* noise while achieving high gain without sacrificing linearity for high performance DCR is one of the critical issues. A method to reduce noise factor of a down-conversion mixer by 5-6 dB and to increase conversion gain by 5-6 dB simultaneously has been proposed. In order to reduce the chip size, on-chip CPW lines has been employed to realize on-chip impedance matching circuits which saves 30-40% chip area than those using the spiral inductors. Finally, RF front-end which consists of on-chip CPW matching circuits, LNA, VCO, and down-conversation mixer has been designed and fabricated on TSMC BiCMOS SiGe 0.35 μm one-poly three-metals technology. A few of the measured results to verify the design theory are presented.

1. INTRODUCTION

As evidence from the recent and rapid growth of 3G cellular phones, wireless LAN, RFID tags, ETC (ETC: Electronic-Toll Collection) systems and so on, there are ever increasing demands of high performance, small size, and high speed microwave devices, circuits, components to meet the existing and future demands of wireless systems [1]-[5]. Therefore, the design of analog circuits has become important in CMOS-LSI technology for not only in optical regime, but also for microwave frequency band. These high-frequency analog LSI circuits (here after RFIC: Radio Frequency Integrated Circuits) design differs from the conventional low-frequency analog circuits because spiral inductors are indispensable in designing amplifiers, mixers, VCOs, or impedance-matching circuits that results in the miniaturization of RFIC components a difficult task. Therefore, the void due to the lack of a new design theory for miniaturization of each component and to reduce numbers of the system components using microwave circuit design rules [6] has been felt for a long time for on-chip realization.

The applications of the distributed elements made of transmission lines were reported in the CMOS or BiCMOS RF-LSI chip [7]-[9]. The CPW lines was exploited as an inductor and used to design a conventional-type matching circuit for an LNA [7] in microwave-band frequency, and they were also used as an inductor in GaAs based monolithic microwave integrated circuit (MMIC) for millimeter-wave devices [8], [9]. However, the application of CPW lines as an inductor takes larger space than a conventional spiral inductor [7]. Some of the present authors have also implemented the CPW superconducting impedance-matching circuit for interconnecting an antenna and duplexer [10], [11] and LSI chips [12], [13].

On the other hand, the direct conversion receiver (DCR) has been attracting much attention in system architecture level due to its simplicity and low cost fabrication of a single-chip realization for wireless transceivers. However, many design issues such as noise, gain, linearity has been critical issues and they are yet to be solved.

The design of mixer is one of the most important steps for high-performance DCR because it involves the issue of flicker (1/*f*) noise and conversion gain simultaneously. CMOS transistors suffer from high 1/*f* noise which is inversely proportional to the device area. So, minimizing 1/*f* noise while achieving high gain without sacrificing linearity for high performance DCR is one of the critical issues. Because of the conversion loss in passive mixers, active mixers are usually preferred in DCR. Among the active mixtures, double-balanced mixers based on the Gilbert cell structure has been widely studied and employed in wireless transceivers.

In this research, we have designed one-chip RF front-end which is composed of LNA, down conversion mixer (DCM), voltage-controlled oscillator (VCO) and (impedance and noise) on-chip matching circuits for WLAN applications (IEEE802.11b). A method to reduce noise figure of DCM and to increase conversion gain without sacrificing linearity has been proposed. Furthermore, a new-type of VCO that employs on-chip

CPW line resonators has been proposed. Finally, one-chip of the designed RF front-end was fabricated on TSMC BiCMOS SiGe 0.35 μm 1-poly 3-metals technology and measured.

2. SYSTEM ARCHITECHTURE AND DESIGN OF EACH COMPONENTS

Fig. 1 shows the block diagram of single chip direct conversion transceiver, which is composed of diode switch, LNA, power amplifier (PA), DCM, and up-conversion mixer (UCM). In the figure, LNA and PA are with input and output matching circuits. The design value of the input impedance and output impedance are 50Ω for general purpose.

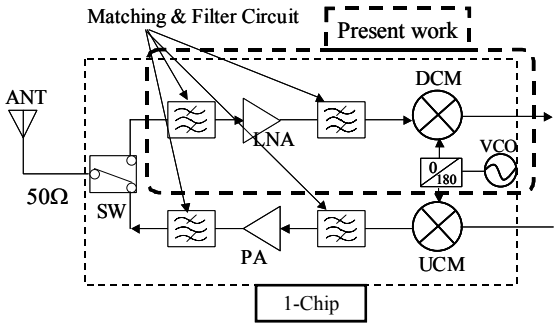


Fig. 1. Block diagram of direct conversion transceiver.

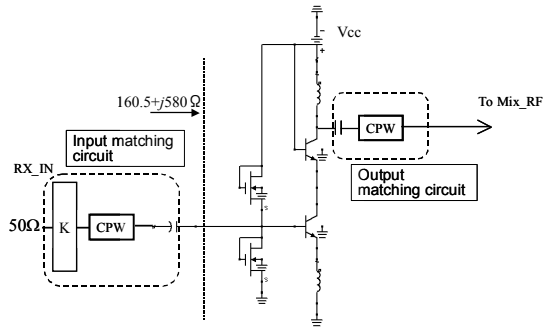


Fig. 2. Schematic of LNA with on-chip matching circuits.

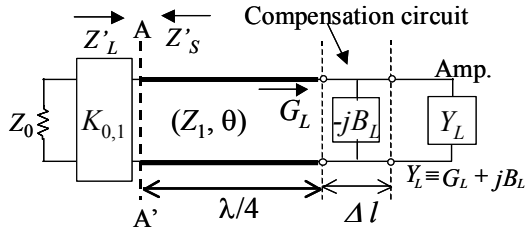


Fig. 3. Circuit model of the proposed matching circuit using λ/4 transmission lines.

2.1 Design of LNA with on-chip CPW matching circuits

Fig. 2 shows the schematic of the designed LNA with on-chip noise and impedance matching circuits. The designed value of the Max gain of the LNA and noise figure (NF) is 19 dB and less than 3dB (@2.45 GHz), respectively. Each V_{CC} and V_{DD} of the 0.35μm BiCMOS process is 3.3V.

The presented matching circuit is based on the theory of the *n*-pole Chebyshev bandpass filter (BPF) [6]. The BPF consists of distributed transmission lines and impedance inverters (*K*-inverters, $K_{i,i+1}$). In usual wireless LAN cards, impedance matching is usually realized by off-chip bonding wires and sometimes on-chip spiral inductors. Realization of matching circuits using off-chip bonding wires is a difficult task because it needs a trial and error process. On the other hand, conventional matching circuit using spiral inductors occupies large on-chip space and it has also encounters self-resonance in microwave frequency band which permits its use beyond that frequency.

Fig. 3 shows the equivalent circuit diagram of the presented matching circuit. Y_L ($=G_L+jB_L$) is the input admittance of the amplifier and Δl is the line length in order to compensate the jB_L. Z_1 and $K_{0,1}$ are the characteristic impedance of the quarter wavelength line and *K* inverter, respectively. The design parameters are given by,

$$\left.\begin{aligned} \Delta\ell &= -\frac{B_L}{\omega_0 C}, \\ Z_1 &= \frac{\pi}{4}\frac{w}{g_1 g_2 G_L}, \\ K_{0,1} &= \sqrt{w}\sqrt{\frac{Z_0 x_1}{g_0 g_1}}, \quad \left(x_1 = \frac{\pi}{4} Z_1\right) \end{aligned}\right\} \tag{1}$$

where, *C* is the capacitance per unit length of the transmission line, and *w* and g_i are the normalized bandwidth and normalized filter element, respectively [6]. The reactance slope parameter (x_1) is for the series resonance circuit. The design parameters of the CPW matching circuit are f_0=2.45 GHz and *w*=100 MHz, which is used as an IEEE 802.11b application.

2.2 Design of Low Noise and High Gain DCM

In DCR architecture, mixer is the main contributor of noise and the overall performance of the receiver is highly affected by the noise performance of mixer. The design of mixer involves the issue of flicker (1/*f*) noise and conversion gain simultaneously. In this research, a highly efficient method to decrease noise factor of a mixer and to increase its conversion gain and linearity, simultaneously is proposed, which will be discussed here after. The 1/*f* component of the output noise current is given as follows [14]:

$$i_{0,n} = \frac{(4I\ v_n)}{(ST_{LO})} \quad (2)$$

$$v_n = \sqrt{\frac{2K_f}{W_{ef} L_{ef} C_{ox} f}} \quad (3)$$

Where T is the LO period, S is the slope of LO signal at switching instant, and I is the bias current of each pair. In a commutating mixer where a large LO amplitude is applied, the low-frequency noise of the switches is resulted. According to Eq. (2), one way of lowering a mixer flicker noise is reducing the width of the noise pulses. This requires the increasing the slope of the LO signal normalized to its frequency [$S.T$], or reducing the flicker noise component of the switching transistors (v_n). The latter is not a good solution because it requires the increasing size of the switches [W_{ef} in Eq. 3]. If W_{ef} is increased, it increases the higher parasitic capacitance at the common source of the switches, resulting in $1/f$ noise indirect translation to the output. On the other hand, LO voltage amplitude is limited to the supply voltage of the signal generator, and increasing its slope at high frequency directly relates to higher power consumption in LO buffers. Furthermore, $1/f$ noise is improved if the height of the noise pulses is decreased. This could be only accomplished by reducing the bias current of the mixer switches as the height of the noise pulses is equal to $2I$.

One of the earliest approaches to reduce the height of the noise pulses is to employ the current injection method at the source terminal of the switching transistors. However, this technique suffers from a few important drawbacks. First, reducing the bias current of the switches raises the impedance seen at their source ($1/g_{ms}$), allowing more RF current to be shunted by the parasitic capacitance at that node. This reduces the mixer bandwidth and degrades linearity. Later, current reuse-scheme is employed to reduce the white noise figure. In this method, the ratio of the injected fixed current to the bias current is usually kept small, improving the switches $1/f$ noise by only a small amount.

In [15], dynamic current injection method has been proposed to inject a dynamic current equal to the bias current of each pair at only the switching event. This is sufficient to eliminate the output flicker noise component completely. In this technique, a dynamic current is injected through a control circuit as shown in Fig. 4 only at the switching event. This effectively reduces the height of the noise pulses at the output to zero and eliminates the flicker noise component. Otherwise no current is injected and the mixer operates normally resulting improvement in power consumption significantly compared to its counterpart such as static current injection method. However, one of the disadvantages of this method is RF signal loss through the control circuits. This problem is overcome by inserting 4 inductors at switching transistors as shown in Fig. 4 and simulated results in Fig. 5 where the simulated performance of the proposed mixer is improved by about 5-6 dB. Noise figure is reduced and conversion gain is improved by equal amount. By introducing four resonating inductors in the switching stage, it also reduces the RF current flowing to the control circuit, thus higher conversion gain is possible at resonant condition.

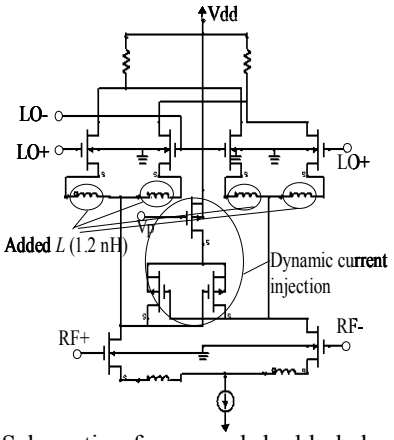
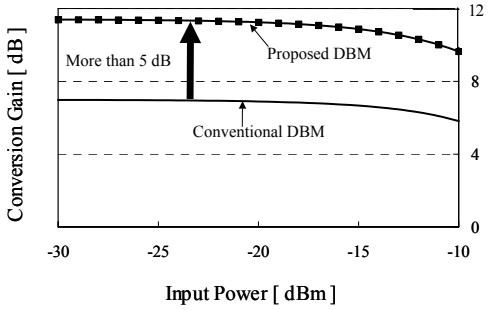
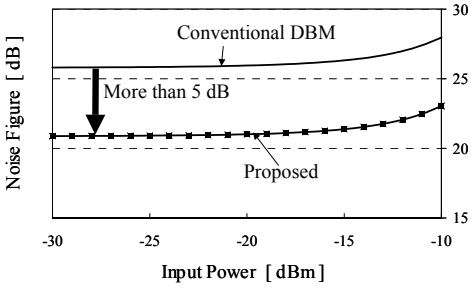


Fig. 4. Schematic of proposed double-balanced mixers using dynamic current injection method and four tuned inductors at switching stage transistors.



(a) Conversion gain improvement



(b) Noise performance improvement

Fig. 5. Simulated performance improvement of the proposed mixture.

2.3 Design of VCO using On-Chip CPW Resonator

A conventional VCO consists of a resonator which is realized by spiral inductors and MIM capacitors (LC resonators) [16]. In this paper, the resonator portion is replaced by on-chip CPW line resonator. Fig. 6 shows structure of CPW resonator on LSI process, where the width of signal line is 5 μm and gap between the line and ground plane is 5 μm. The length of the resonator is 6700 μm so that its resonant frequency is to be 2.4 GHz under the given parameters of LSI process.

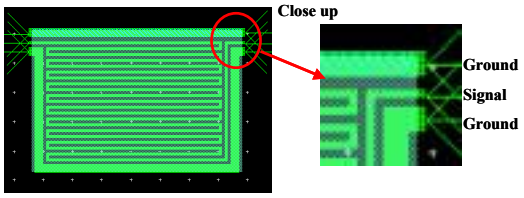


Fig. 6. Structure of CPW resonator on LSI process.

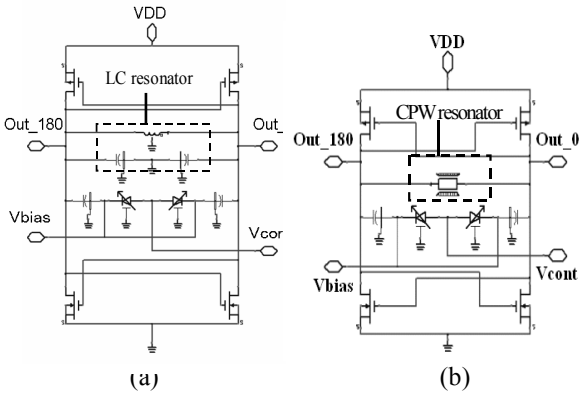


Fig. 7. Schematics of designed VCO using (a) LC resonator (b) proposed CPW resonator.

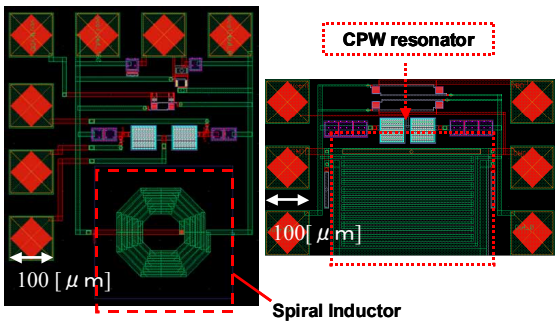


Fig. 8. Layout of the designed VCO using (a) LC resonator (b) proposed CPW resonator.

Fig. 7 shows the schematics of the designed VCO. In the design, widely used CMOS cross-coupled structure is used. In Fig. 7(a), the VCO using LC resonator is shown and that of using the proposed CPW resonator is shown in Fig. 7(b). Layouts of both VCO are shown in Fig. 8. One of the advantages of using CPW resonators is that it takes 30% less on-chip space than that of a conventional VCO using LC resonator.

The comparison of simulated parameters between the VCOs using CPW resonator and LC resonator is shown in Table 1. From the table, it is noted that the VCO using CPW resonator has advantages in terms of chip area and frequency turning range (FTR). On the other hand, it has the adverse performance in terms of consumption power and phase noise.

Table 1. Comparison of simulated parameters between two VCOs. [FTR=frequency tuning range]

	LC resonator	CPW resonator
Amplitude [V]	1.6	1.0
Centre [GHz]	2.456	2.789
FTR [%]	10	24
Consumption power [mW]	15.5	44.6
Phase noise [dBc/Hz]	-126	-118
Area $[m^2]$	2.2×10^{-7}	1.8×10^{-7}

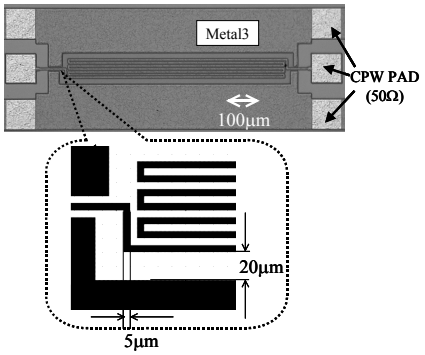


Fig. 9. Chip photo of conductor backed CPW.

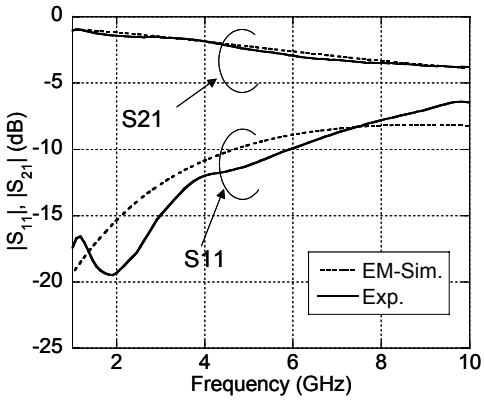


Fig. 10. Frequency responses of the CPW meanderline.

3. FABRICATED CHIP AND MEASURED RESULTS

3.1 CPW Line Structure and Losses

K-inverter is fabricated using shunt meander structure so that they can be used to exploit the vacant space inside the chip. Fig. 9 shows a photo of CPW line circuits. The conductance of the metal is 4.1×10^7 S/m. The signal width and the interval between the slots of the CPW transmission line are 5 μm and 15 μm, respectively. Fig. 10 shows the comparison of the frequency responses of the *K*-inverter. Insertion loss (S_{21}) of the EM-simulated result is almost in agreement with that of the experimental result.

Fig. 11 shows the microphotograph of a single-chip LNA and DCM for 2.4 GHz-band wireless LAN applications, and the proposed impedance-matching circuit interconnecting between them and at the input of the LNA.

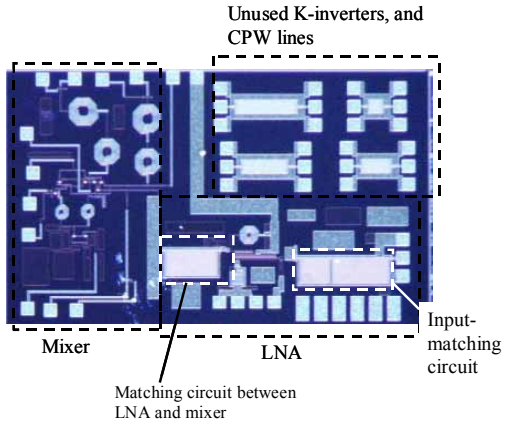


Fig. 11. Microphotograph of SiGe BiCMOS reciever front-end. (Chip size: 2mm x 3.5 mm)

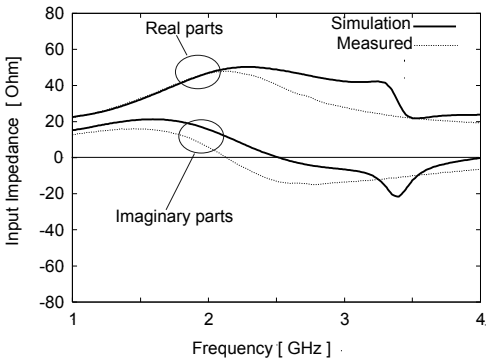


Fig. 12. Input impedance of the designed chip.

Fig. 12 shows the comparison of the measured and simulation results of the input impedance of the fabricated chip. In the figure, the measured results are in good agreement with the designed value. For example, the measured real part of the input impedance is about 47 Ω compared with 50 Ω of the designed value (@2.45 GHz). Similarly, the measured imaginary part is about –9 Ω compared to the +2 Ω of the designed value.

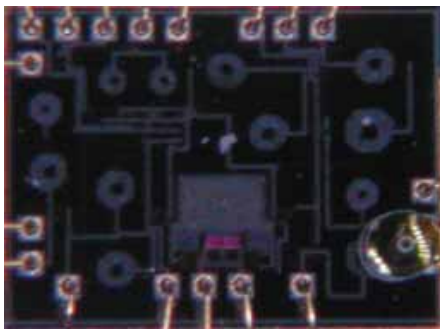


Fig. 13. Chip photo of proposed mixer connected with proposed VCO using CPW resonator. (Chip size =1.3 mm x 1.7 mm including the matching circuits and biasing circuits at RF terminal).

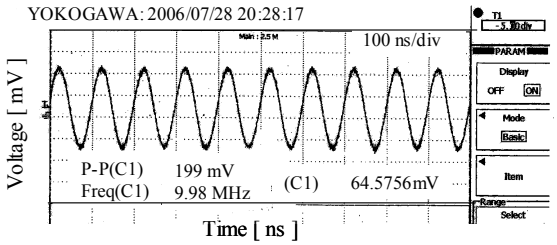


Fig. 14. Output of mixer sinusoidal waveform confirming the operation of the mixer measured by digital oscilloscope through a high-impedance probe (IF frequency =10 MHz).

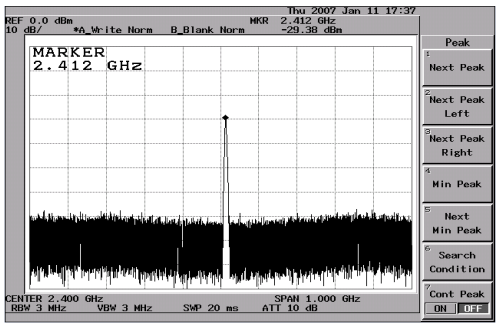


Fig. 15. An example of VCO output measured by spectrum analyzer.

Fig. 13 shows a chip photo of proposed down conversion mixers and its measured results in time domain is shown in Fig. 14. This shows the operation of the fabricated mixer. Similarly, Fig. 15 shows the measured results of proposed VCO which confirms of

its operation. The detail measurement results will be presented in future study.

4. CONCLUSION

RF front-end which consists of integrated on-chip CPW line impedance and noise matching circuits, LNA, down conversion mixer and VCO is designed and fabricated on TSMC 0.35 μm SiGe BiCMOS process. An effective method to reduce noise figure and simultaneously to increase conversion gain of the mixer without sacrificing linearity and consumption power has been proposed. In order to reduce the chip size for on-chip realization, on-chip CPW lines has been employed to realize on-chip impedance and noise matching circuits which saves 30-40% chip area than those using the spiral inductors. Some of the preliminary measured results of each element of the chip have been presented. Improvement of phase noise and consumption power of VCO is one the most important issues which is to be solved in near future.

ACKNOWLDGEMENT

This work is supported by VLSI Design and Education Center (VDEC), The University of Tokyo with the collaboration with Agilent Technologies and Cadence Corporation.

REFERENCES

[1] A. Matsuzawa, “RF-SoC-expectations and required conditions”, IEEE. Trans. Microwave Theory Tech., vol. 50, no. 1, pp. 245-253, January 2002.

[2] M. S. J. Steyaert, G.D. Muer, P. Leroux, M. Borremans, and K. Mertens, “Lov-Voltage Low-Power CMOS-RF Transceiver Design”, IEEE. Trans. Microwave Theory Tech, vol. 50, no. 1, pp. 281-287, January 2002.

[3] T. H. Lee, H. Samavati, and H. R. Rategh, “5-GHz CMOS Wireless LANs”, IEEE. Trans. Microwave Theory Tech., vol. 50, no. 1, pp. 268-280, January 2002.

[4] D. L. Harame, D. C. Ahlgren, D. D. Coolbaugh, J. S. Dunn, G. G. Freeman, J. D. Gillis, R. A. Groves, G. N. Hendersen, R. A. Johnson, A. J. Joseph, S. Subbanna, A. M. Victor, K. M. Watson, C. S. Webster, and P. J. Zampardi, P.J., “Current status and future trends of SiGe BiCMOS technology,” IEEE. Trans. Electron Device, vol. 48, no. 11, pp. 2575-2594, November 2001.

[5] O. Shana, I. Linscott, and L. Tyler, “Frequency-Scalable SiGe Bipolar RF Front-End Design”, IEEE Journal of Solid-State Circuit, vol.36, no. 6, pp. 888-895, June 2001.

[6] G. L. Matthaei, L. Young and E. M. T. Jones, Microwave Filters, Impedance-Matching Networks, and Coupling Structures. Norwood, MA: Artech House. 1980.

[7] M. Ono, N. Suematsu, S. Kubo, K. Nakajima, Y. Iyama, and O. Ishida, “Si substrate resistivity design for on-chip matching circuit based on electro-magnetic simulation”, IEICE Trans. Electron., vol. E84-C, no. 7, pp. 923-929 July 2001.

[8] Y. Umeda, T. Enoki, and Y. Ishii, “Sensitivity analysis of 50-GHz MMIC-LNA on gate recess depth with InAlAs/InGaAs/InP HEMTs”, IEEE MTT-S Int. Microwave Symp. Dig., pp.123-126, 1994.

[9] C. Rheinfelder, K. Strohm, F. Beisswanger, J. Gerdes, F. J. Schmuckle, J.-F. Luy, and W. Heinrich, “26 GHz coplanar SiGe MMICs,” IEEE MTT-S Int. Microwave Symposium, Dig. 1, pp. 273-276, June 1996.

[10] K. Yoshida, T. Takahashi, H. Kanaya, T. Uchiyama, and Z. Wang, “Superconducting slot antenna with broadband impedance matching circuit,” IEEE Trans. Appl. Supercond., vol. 11, no. 2, pp. 103-106, June 2001.

[11] Y. Tsutsumi, H. Kanaya, and K. Yoshida, “Design and performance of an electrically small slot loop antenna with a miniaturized superconducting matching circuit”, *IEEE Trans. Appl. Supercond.*, vol. 15, no. 2, pp. 1020-1023, June 2005.

[12] H. Kanaya, R. K. Pokharel, F. Koga, D. Arima, S. Kim, and K. Yoshida, "Design of Coplanar Waveguide On-Chip Impedance-Matching Circuit for Wireless Receiver Front-End," 2006 IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium, paper no. 1229, San Francisco, June 2006.

[13] H. Kanaya, R. K. Pokharel, F. Koga, and K. Yoshida, "Design and Verification of On-Chip Impedance-Matching Circuit Using Transmission-Line Theory for 2.4 GHz-Band Wireless Receiver Front-End," IEICE Trans. on Electron., Vol. 89-C, no. 12, pp. 1888-1895, Dec. 2006.

[14] H. Darabi and A. Abidi, “Noise in RF-CMOS mixers: A simple physical model,” IEEE Transactions on Solid State Circuits, pp. 15-25, vol. 35, no. 1, Jan. 2000.

[15] H. Darabi and J. Chiu, “A noise cancellation technique in active RF-CMOS mixers,” IEEE Journal of Solid-State Circuits, vol. 40, no. 12, pp. 2628-2632, Dec. 2005.

[16] B. Razavi, “Design of analog CMOS integrated circuits,” McGraw-Hill Education, 2000.