A 3.1 – 4.8 GHz CMOS UWB Power Amplifier Using Current Reused Technique

S.A.Z. Murad, R.K. Pokharel, H. Kanaya and K. Yoshida

Graduate School of Information Sciences and Electrical Engineering,
Kyushu University,
Fukuoka 819-0395, Japan.
murad@yossvr3.ed.kyushu-u.ac.jp

Abstract— **This paper describes the design of a 3.1 to 4.8 GHz CMOS power amplifier (PA) for ultra-wideband (UWB) applications using TSMC 0.18-µm CMOS technology. The UWB PA proposed in this paper employs cascode topology with an additional common source stage to achieve high power gain. The current reused technique is implemented to enhance the gain at the upper end of the desired band for gain flatness and the resistive feedback at the second stage is used to improve wideband matching. The post-layout simulation results indicate that the gain at the upper end of desired frequency is increased about 11 dB and the gain flatness of 18.4±1 dB is achieved, improved the linearity at an input 1-dB compression point of -10.6 dBm, and consumes low power (22 mW) at 1.0 V DC supply voltages.**

Keywords-power amplifier; ultra-wideband; cascode; current reused; low power

I. INTRODUCTION

At present time, the wireless connection becomes popular in a lot of new communication systems. Ultra-wideband (UWB) system is one of the new communication systems, which are able to transmit data over a wide spectrum of frequency bands from 3.1 to 10.6 GHz with very low power and high data rates [1]. This new technology has attracted many researchers in both academic and industrial to exploit this higher data rate and wider bandwidth wireless applications in comparison to others technology such as Bluetooth and WiMAX. The possible applications of UWB technology can be applied in sensor networks, imaging systems, wireless personnel area network (WPAN) and so on.

The design of UWB power amplifier (PA) is a key part of the RF front-end in any transmitter because it is a very power hungry. However, in UWB systems, the power level from the UWB transmitter should be small enough not to interfere with the already existing communication systems [2]. This mandates the use of low output power levels is limited at -41.25 dBm/MHz (as specified by the FCC). Therefore, the small transistors as part of the PA circuit are desired for consuming less power consumption. However, achieving a high gain and good impedance match over the entire frequency band makes the design a challenging task. There is a trade-off between efficiency, linearity and gain requirement in designing UWB PA.

Recently, wireless devices are becoming more and more popular in many applications and the need to build compact, low cost and low power blocks arises. In addition, more and more signal processing is done in CMOS. Therefore, CMOS technology had been implemented in much transceivers design for a lot of applications. However, as the down-scaling of MOS devices continues, the CMOS PA is not the optimum technology of choice due to the problem such as low oxide breakdown voltage, low current drive capability, substrate coupling and low quality and high tolerances of on chip passives [3][4]. This makes CMOS PA design and implementation a major challenge, particularly when designing in GHz frequencies range.

In this paper, a low frequency band CMOS power amplifier from 3.1 to 4.8 GHz for UWB applications is presented. Since the output power level of UWB signals must be too low in order to match the power mask of FCC [1], the proposed design only focused on bandwidth, linearity and power consumption of the UWB PA. Using cascode topology with additional common source allows increasing power gain. The current reused technique helps to achieve gain flatness by enhance the gain at the upper end of the desired band. The wideband matching is improved by resistive shunt feedback at the second stage and inductance source degeneration obtains the stability of the amplifier. The separate grounding between the first stage amplifier and the second stage amplifier reduces the gain sensitivity.

II. CIRCUIT DESIGN

There are many topologies have been implemented to realize wideband PA. Distributed amplifier [5], RLC matching topology [6], and resistive shunt feedback [7] have been reported for broadband PA. Distributed amplifier can provide good matching and linearity over a wideband of frequencies; however, the power consumption and the chip area can be quite high in these circuits. RLC matching also can provide wideband matching and consume less power consumption, but it often needs a number of reactive elements to form the wideband bandpass filter, therefore, occupy large area of a chip and complicated in the layout design as well.

In contrast, resistive shunt feedback can provide the wideband matching at both input and output ends. This topology has the added advantage of providing stability [7]. Recently, current-reused technique proposed in UWB low

978-1-4244-3693-4/09/$25.00 ©2009 IEEE

noise amplifier has been successfully enhancing the gain at the upper end of the desired band [8], [9].

Therefore, the current reused technique is employed to improve gain flatness and the resistive shunt feedback is implemented for wideband matching [10]. The theoretical analysis about current reused technique can be found in [9], [11]. The source degeneration inductor is realized by bonding wires to achieve good stability for amplifier.

The proposed design of UWB PA circuit can be divided into three parts as shown in Fig. 1. The first part consists of current reused cascoded common source (CS) structure, where the M1 and M2 are two CS amplifiers. M2 is also CS amplifier converting from a common gate (CG) amplifier by the current reused technique. The impedance of L_{D1} is adequately large to provide a high impedance path to block the signal at the desired bandwidth, while the C_{G2} and L_{G2} of M2 provide a low impedance path. Therefore, the input signal can be amplifier twice under this technique. A narrow band characteristic composed by the resonate circuit of C_{G2} and L_{G2} is employed to enhance the gain at the upper end of the desired band. In addition, L2 is inductive peaking to achieve high gain at higher frequency. Capacitor C_{DC} is DC blocking and inductor Lin is part of the input matching, while L1 is source degeneration realizing using bondwires. Cbp is the bypass capacitor, and Rb is the bias resistor of M2. M1 is biased in class AB to achieve sufficient linearity and efficiency.

The second stage consists of inter-stage inductor Lis, and inter-stage capacitor Cis, for matching purpose between the first stage and the second stage amplifier and also to improve the gain. The third stage is CS amplifier with resistive shunt feedback Rf to obtain wideband matching. L3 is a load for CS amplifier of M3 realizing using bondwire. Inductor Lo is used to achieve output matching. It should be finally noted that the effect of bondwires was taken into account during simulations (L1, L3 and L4 in Fig. 1). These bondwires are well defined and modeled accurately with physical lumped element models by using Cadence SpectreRF.

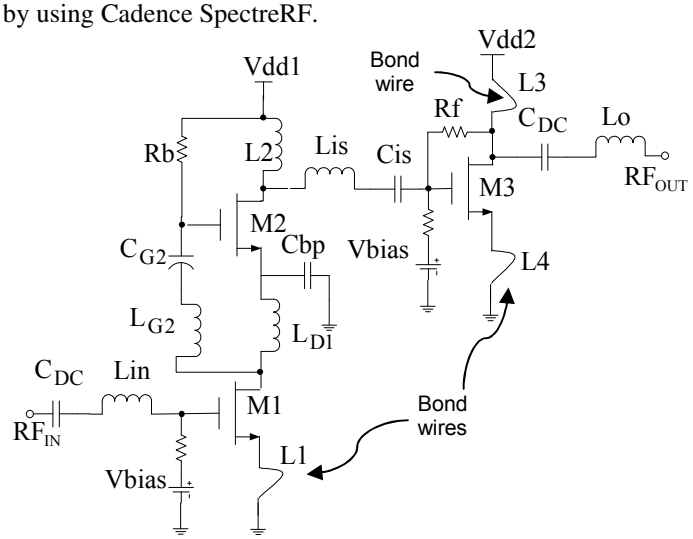

Figure 1. Schematic of the proposed current reused UWB PA.

III. Simulation Results

The circuit design of the UWB PA is simulated using Cadence SpectraRF simulator in TSMC 0.18-μm CMOS process. Fig. 2 shows the simulated small signal gain using S-parameter analysis for pre-layout and post-layout. The gain at the upper end of a desired band, 4.8 GHz is increased to compare with the circuit without employed current reused technique. Therefore, this technique helps to improve the gain approximately about 11 dB at the upper end of the desired frequency 4.8 GHz; and the gain flatness of 18.4±1 dB is achieved between the operation frequencies' ranges. The pre-layout simulation and post-layout simulation results match well at the frequency ranges of interest.

The simulated input and output return loss, S11 and S22 are plotted in Fig. 3. The return loss at the input and output is below than -5 dB within the required bandwidth is achieved.

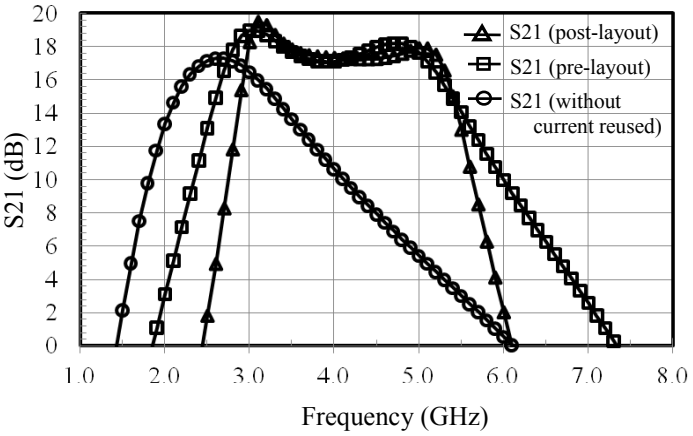

Figure 2. Simulated gain without current reused and with current reused (pre-layout and post-layout) of UWB PA.

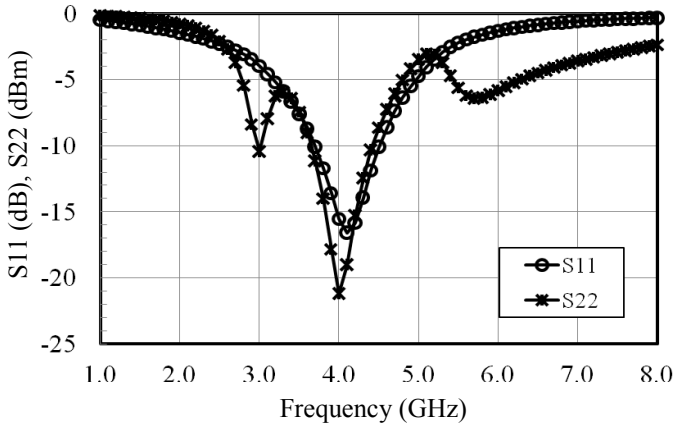

Figure 3. Simulated input and output return loss of UWB PA (post-layout).

The gain is a major performance merit for a power amplifier; however, the linearity is also important. The linearity limits the actual power that can be driven to the load by the PA [6]. The PA can drive the wanted signal without too many harmonic terms only in linear region operation. The linearity of the PA is simulated using a periodic steady state (PSS). The 1-dB compression at -10.6 dBm for a 4 GHz and the PA delivers

an output power of 6.0 dBm at this point as shown in Fig. 4. The 1-dB compression point between -14.5 dBm to -10.5 dBm is obtained between 3.0 to 5.0 GHz.

Fig. 5 shows the simulated output power (Pout) and power added efficiency (PAE) vs. input power (Pin) at 4 GHz. The output power and PAE are about 6.0 dBm and 18%, respectively at -10.6 dBm input power. The stability of the proposed UWB PA as shown in Fig. 6 is unconditionally stable because the stability factor (K-factor) more than one is obtained for the whole frequencies.

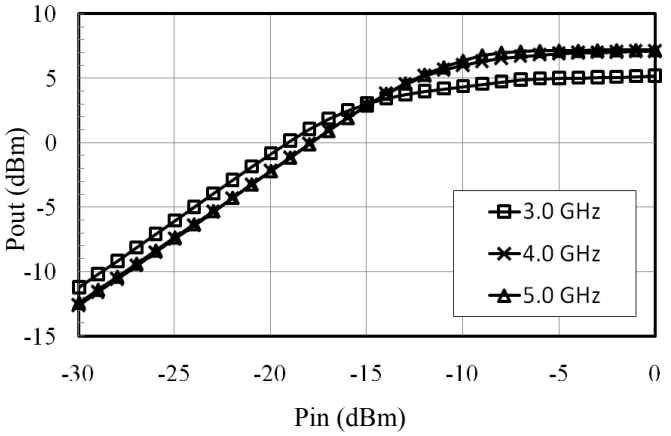

Figure 4. Simulated 1-dB compression point of UWB PA (post-layout).

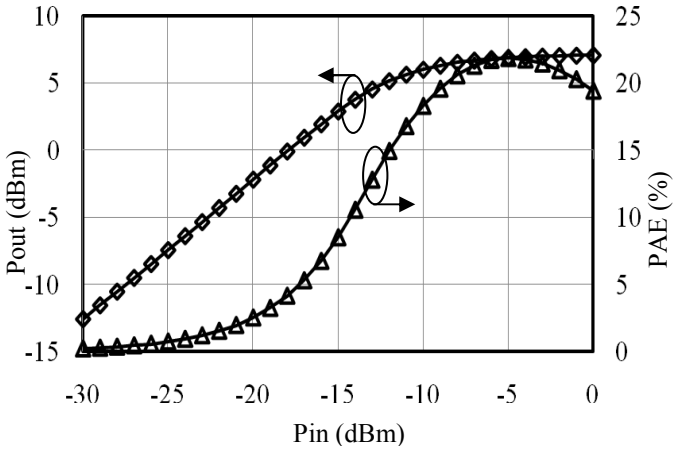

Figure 5. Simulated output power and PAE of UWB PA (post-layout).

Table 1 shows the comparison of performances of the previously reported UWB PA and this work. Reference [7] was proposed to employ a cascode configuration and series R-C feedback network for gain flatness and wideband matching, however the linearity and PAE were very poor. In [11] design was implemented two-stage cascaded configuration with shunt-shunt feedback to obtain the higher gain and ultra wide bandwidth, but the linearity and power consumption was not measured and the performance of PAE was also low.

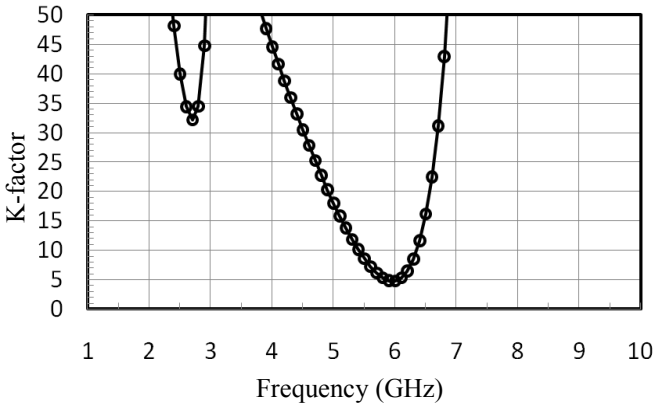

Figure 6. Simulated K-factor for stability of UWB PA (post-layout).

In [12] was proposed double-stage PA (cascode topology with additional CS stage) wideband inductive degeneration resistive feedback power amplifier, however the input and output return loss was very poor and consuming huge power. Reference [13] was designed UWB PA employs inter-stage wideband impedance transformer for the wideband operation at the difference frequency ranges of interest. The proposed design performance was achieved good wideband matching, linearity, high PAE and low power consumption but with the low power gain.

In contrast, the proposed design in this work obtained good gain flatness, high linearity and low power performance when compare with the previous worked at the same frequency ranges of interest. However, two inductors are needed for realizing current reused technique, which can increase the chip size area, but active inductors can be employed to reduce the chip size. The layout of the proposed UWB PA is presented in Fig. 7. The die area including the pads is 0.95 mm × 1.02 mm; this layout is going to tape out for fabrication soon.

IV. CONCLUSIONS

A 3.1 – 4.8 GHz CMOS power amplifier using current reused technique has been designed and simulated in the TSMC 0.18-µm CMOS process. The proposed UWB PA provides wide bandwidth, good gain flatness, high linearity and low power consumption that can be implemented for UWB applications. The cascade with an additional common source stage topology is used to achieve high gain. The gain flatness is clearly achieved at the desired frequency by using current reused technique while resistive feedback at the second stage amplifier providing wideband matching. The simulation results show that the PA achieves a gain flatness of 18.4±1 dB with an output power of 6.0 dBm at an input 1-dB compression point at -10.6 dBm. The designed PA consumes low power about 22 mW at 1.0 V DC supply voltages with the chip size is about 0.97 mm². This proposed design can be extended for uses up to 10.6 GHz in the future due to the characteristic of current reuse technique that can enhance the gain at the upper end of the desired band.

TABLE I. SUMMARY AND COMPARISON OF UWB PA PERFORMANCES

Reference	[7] [a]	[12] [b]	[13] [a]	[14] [b]	This work[c]
Technology (μm)	0.18	0.18	0.18	0.18	0.18
Supply voltage (V)	1.8	-	1.9	1.5	1.0
Frequency (GHz)	3.1-4.8	3-5	3.1-4.8	6-10	3.1-4.8
S11(dB)	<-10	<-10	<-4.6	<-7	<-5
S22 (dB)	<-8	<-10	<-1.3	<-7	<-5
Gain (dB)	19±1	17.5-21	22.3-25.5	8.5	18.4±1
Input P_{1dB} (dBm)	-22 @ 4 GHz	-	-17 @ 4 GHz	-	-10.6 @ 4 GHz
Output P_{1dB} (dBm)	-4.2 @ 4 GHz	0.42 @ 4 GHz	-	5.0	6.0 @ 4 GHz
PAE (%)	1.5 [d] @ 4 GHz	3.9 @ 4 GHz	-	14.4	18.0 @ 4 GHz
Power consumption (mW)	25	-	26.7	18	22
Chip size (mm^2)	2.09	1.52	2.04	1.08	0.97

a. Pre-layout simulation result

b. Measurement result

c. Post-layout simulation result

d. Estimated value [12]

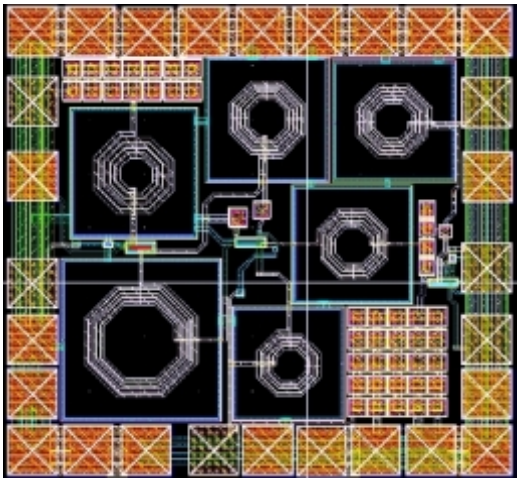

Figure 7. Layout of the proposed UWB PA on 0.18-μm CMOS technology.

ACKNOWLEDGMENT

This work was partly supported by a grant of Knowledge Cluster Initiative implemented by Ministry of Education, Culture, Sports, Science and Technology (MEXT) and KAKENHI. This work was also partly supported by VLSI Design and Education Center VDEC), the University of Tokyo in collaboration with CADENCE Corporation and Agilent Corporation.

REFERENCES

[1] FCC (2002), First Report and Order. [Online]. Available: http://www.fcc.gov/Bureaus/Engineering_Technology/Orders/2002/fcc02048.pdf

[2] S. Jose, "Design of RF CMOS power amplifier for UWB application," Msc. in Electrical Eng. thesis, Virginia Polytechnic Institute and State University, Virginia, USA, Dec. 2004.

[3] A.Mazzanti, L.Larcher,R.Brama & F.Svelto, "Analysis of reliability & power efficiency in cascode class-E PAs," IEEE Journal of Solid-State Circuits, Vol. 41, No.5, May 2006.

[4] Tirdad Sowlati & Domine M.W. Leenaerts,"A 2.4 GHz 0.18um CMOS self-biased cascode PA," IEEE Journal of Solid State Circuit, Vol.38, No. 8, August 2003.

[5] C.Grewing, K. Winterberg, S.V. Waasen, "Fully integrated distributed power amplifier in CMOS technology, optimized for UWB transmitter," IEEE RF IC Symposium, Aug. 2004.

[6] Han Chou Hsu, Zhi Wei Wang & Gin Kou Ma, "A low power CMOS full-band UWB power amplifier using wideband RLC matching method," IEEE Conference on Electron Devices and Solid-State Circuits , pp. 233-236, 19-21 Dec. 2005.

[7] S. Jose, H.J Lee & D. Ha, "A low power CMOS PA for UWB applications," IEEE Int. Symposium on Circuits & Systems, ISCAS 2005, vol. 5, pp. 5111-5114, 23-26 May 2005.

[8] Z.D. Huang, Z.M. Lin, and H.C. Lai, "An hihg gin low noise amplifier with current-reused technique for UWB applications," IEEE Conference on Electron Devices and Solid-State Circuits, pp. 977-980, 20-22 Dec. 2007.

[9] Yi-Jing Lin, Shawn S.H. Hsu, Jun-De Jin, and C.Y. Chan, "A 3.1- 10.6 GHz ultra-wideband CMOS low noise amplifier with current-reused technique," IEEE Microwave and Wireless Components Lett., vol. 17, no. 3, pp. 232-234, March 2007.

[10] R.K Pokharel, A.I.A. Galal, O.Nizhnik, H. Kanaya, and K. Yoshida, " Design of flat gain and low noise figure LNA for 3.1-10.2 GHz band UWB applications in 0.18 μm CMOS process," IEEJ International Workshop on AVLSI, pp. 161-164, 2008.

[11] H.L.Kao, K.C Chang, "Very low-power CMOS LNA for UWB wireless receivers using current-reused topology", Solid-State Electronic, Vol. 52, Issue 1, January 2008.

[12] Ruey-Lue Wang, Yan-Kuin Su, Chien-Hsuan Liu, "3~5 GHz cascoded UWB power amplifier," IEEE Asia Pacific Conference on Circuits and Systems 2006, pp. 367 – 369, 4-7 Dec. 2006.

[13] Maisurah, S. Wong Sew Kin Kung, F. See Jin Hui, "0.18 μm CMOS power amplifier for ultra-wideband (UWB) system," in IEEE International Conference on Wireless and Optical Communications Networks , pp. 1-4, 2-4 July 2007.

[14] H.-W Chung, Hsu, C.-Y., Yang, C.-Y, Wei, K.-F., Chuang, H.-R., "A 6-10-GHz CMOS power amplifier with an inter-stage wideband impedance transformer for UWB transmitters," 38th European Microwave Conference , pp. 305-308, 27-31 Oct. 2008.