2009/3/27～2009/4/3

Introduction of Fabless Methodology in Electronics by EDA Tools and Foundries

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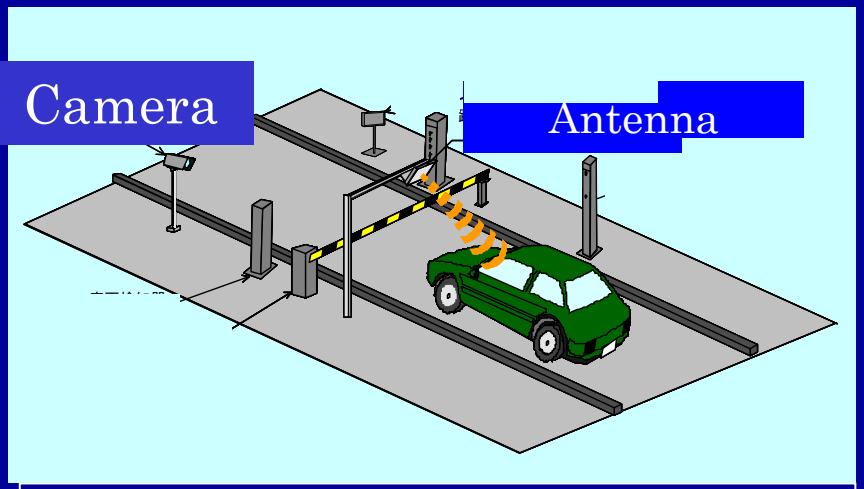
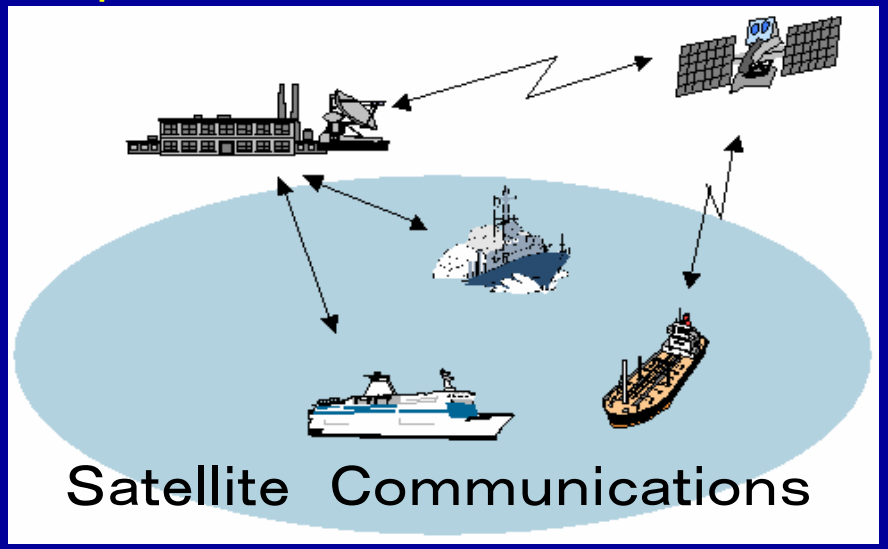
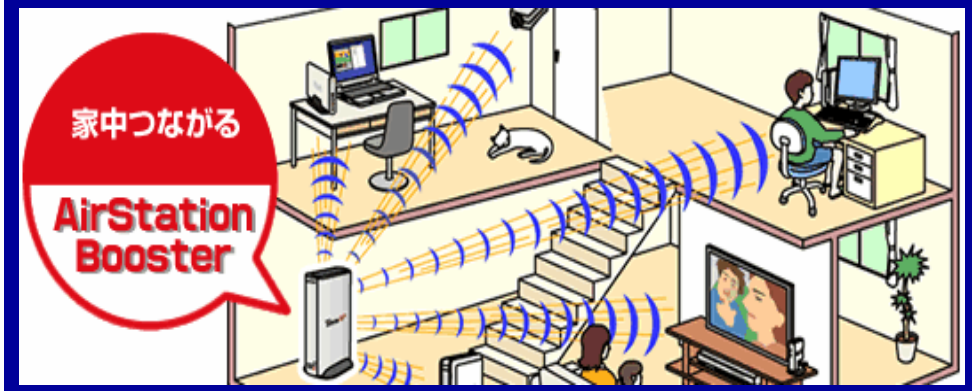
Driving Force: Wireless Technologies

Wireless LAN、Cell Phone、Cordless Telephone、IC Card, ITS, DSRC



Electronic-Toll Collection System.



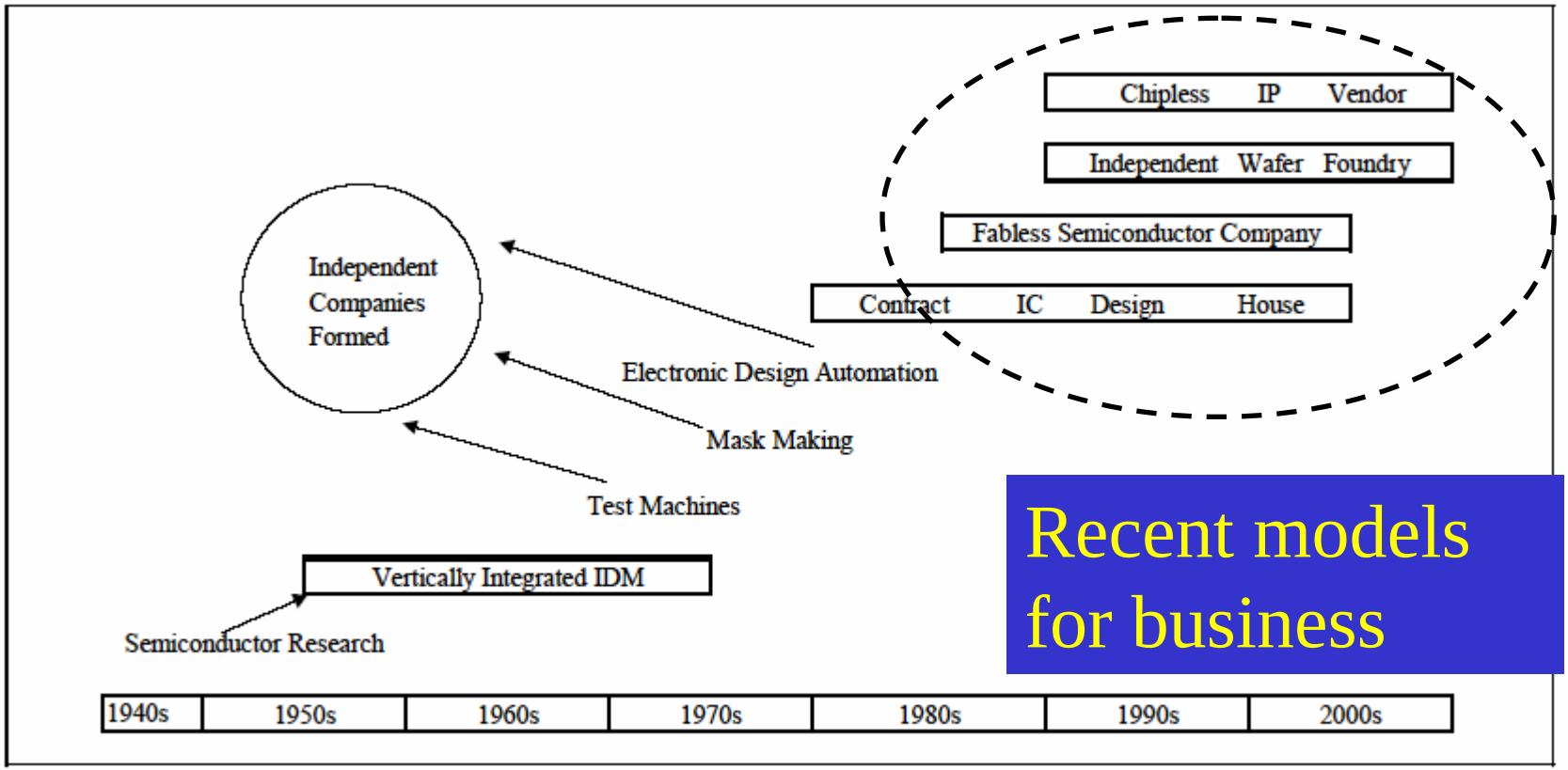


Wireless LAN

Cell Phone

Cordless Phone

The Design House Phenomenon



Recent models for business

Source: Future Horizons

Fabless Company-Designs IC at home and outsource the fabrication.

IC Insights top 20 rankings in 2008

Fabless Design Model still prosper for 30-40 years

2008 Top 20 Semiconductor Sales Leaders ($M)

2008 Rank	2007 Rank	Company	Headquarters	2007 Tot Semi	2008 Tot Semi	2008/2007 % Change
1	1	Intel	U.S.	35,021	34,490	-2%
2	2	Samsung	South Korea	19,951	20,272	2%
3	3	TI	U.S.	13,309	11,966	-10%
4	4	Toshiba	Japan	11,850	11,059	-7%
5	5	TSMC*	Taiwan	9,813	10,556	8%
6	7	ST**	Europe	8,637	9,052	5%
7	8	Renesas	Japan	8,001	7,017	-12%
8	13	Qualcomm***	U.S.	5,619	6,477	15%
9	9	Sony	Japan	7,203	6,420	-11%
10	6	Hynix	South Korea	9,201	6,182	-33%
11	12	Infineon	Europe	5,772	5,972	3%
12	11	AMD	U.S.	6,013	5,808	-3%
13	14	NEC	Japan	5,593	5,732	2%
14	15	Micron	U.S.	5,520	5,688	3%
15	10	NXP	Europe	6,026	5,318	-12%
16	16	Freescale	U.S.	5,447	4,898	-10%
17	23	Broadcom***	U.S.	3,754	4,509	20%
18	17	Fujitsu	Japan	4,568	4,462	-2%
19	21	Panasonic	Japan	3,810	4,321	13%
20	19	Nvidia***	U.S.	3,979	3,660	-8%
—	—	Total Top 20	—	179,087	173,859	-3%

*Foundry **Not incl. flash and ST-NXP Wireless in 2007 & 2008 ***Fabless

Source: Company reports, IC Insights

Fabless vendor

Even in the worst downturns,
Fabless company and Fabless vendor ⇒ High growth rates

Scope & Trend

Intel (USA),
Samsung (Korea),
TI (USA) etc.

Vertically integrated (1980s)

- Owned and operated their own silicon wafer fabrication plant.
- Developed their own process technology.
- Performed assembly and test for their chips.

Technology node Running cost

EDA: CAD Tools

Collaboration

Horizontal (international) specialization

Fabless (LSI Deign)

LSI Design only, First TAT, New company, Venture company
Necessity of research and development resources for LSI Design

Foundry (LSI fabrication)

Have a deep sub-micron semiconductor fabrication p
(Fabless Vendor)

Vision of E-JUST

Foundry for Integrated Circuits (ICs)

GaAs, GaN, InP, SiC, SiGe, SOI, CMOS

Trade-off between NF, cost, performance, frequency of applications and so on.

Comparison between GaAs and CMOS

GaAs :

--Low noise at higher frequencies

--Faster switching speed

-- High cost

CMOS:

-- Low cost

-- SiO_2 is one of the best insulators

-- Hole mobility that leads to fabricate P-MOSFET for CMOS logic (digital circuits).

SOI: Silicon on Insulator

--Layered silicon-parasitic capacitances-performance improvement

--Hole mobility reduces

RF-MEMS (RF Microelectromechanical Systems)

Applications in RF-LSI: **Switches, switched capacitors and varactors, high Q-inductors**

Other Applications are antennas, tunable filters and phase shifters.

Recent trend is in Digital RF processor—using no inductors in RF front end.

Japanese Trends in RF-MEMS

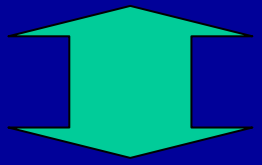
Industry

Academia

In Japan-Integrated MEMS (MEMS + CMOS) Research Society was established on 2008 (one year before).

Slogan: More than Moore by True MEMS

Success in LSI???



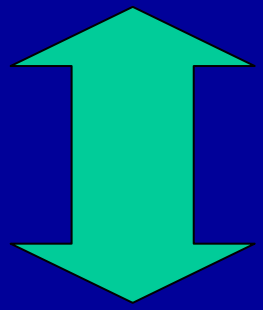
Reason: Digital RF Processor

Our Private Opinion

RF-MEMS should compete with Digital RF Processor

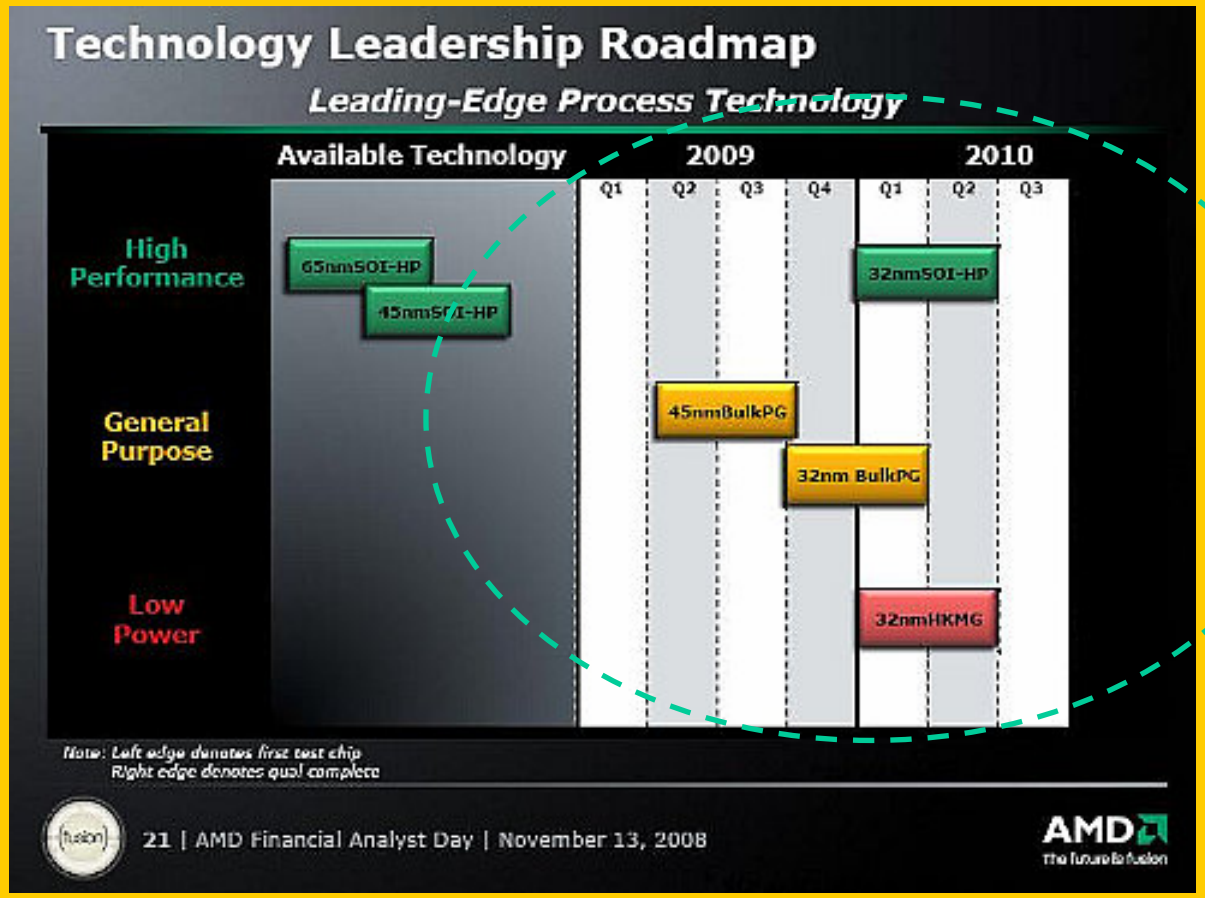
Who will be the winner?

Guess: Digital RF Processor due to low cost



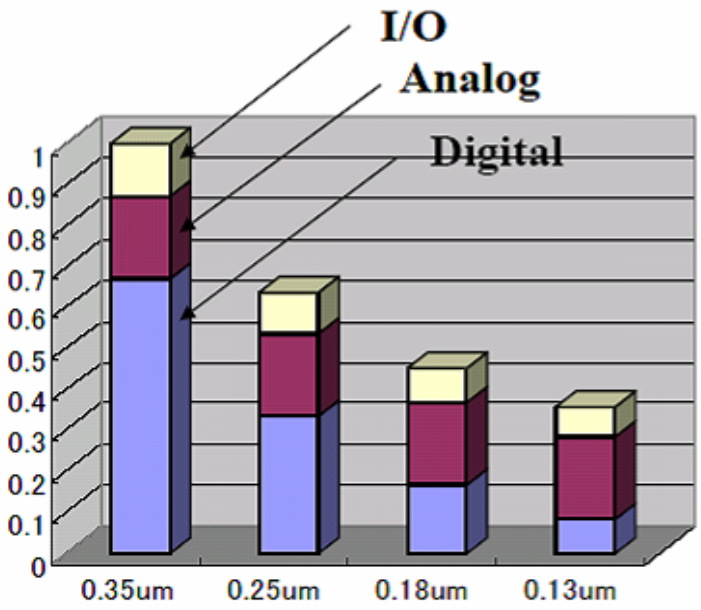
CMOS is best solution for
university level research.

Roadmap of CMOS Technologies

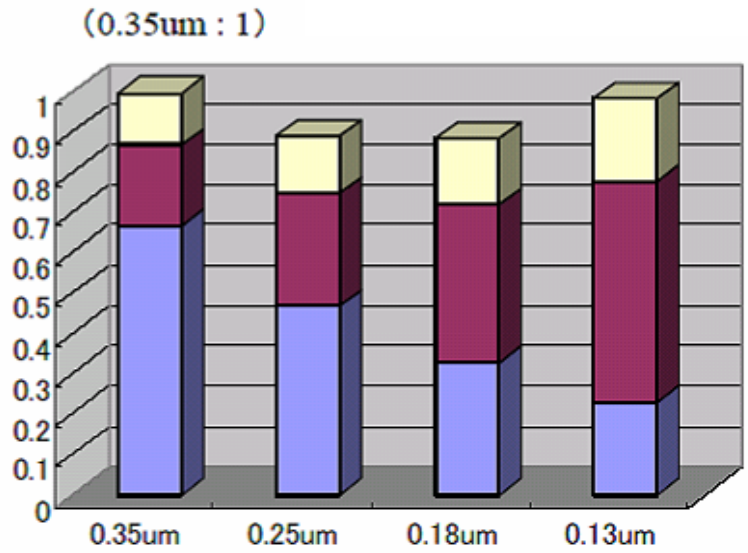


Only logic

Comparison between Digital and Analog



Chip area



Chip cost

High Cost of Conventional Analog Circuits

Spiral Inductors—Does not reduce with deep sub-micron CMOS

Foundry Cost

Shuttle Service- TWO WAYS in Japan

Through VDEC

Through private companies

We use this option.

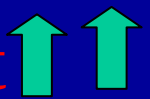
Chip COST (in ¥)

CMOS 0.18um Mixed signal	2.5M (+Packaging)
CMOS 90nm Mixed signal	5M (+Packaging)
CMOS 65nm Mixed signal	7.5M (+Packaging)

5mm x 5mm
(Chip size)

Foundry at University Level Research

- 0.18 um CMOS : Because it is cheaper and academic discount is available.
- Applications: below 12 GHz
  - ✓ Ultra-wideband (UWB) applications
  - ✓ Multi-standard systems
  - ✓ Software-defined radio or so on.

Millimeter-wave applications: 90 nm CMOS but cost 

Cost Estimation for Fabrication (Material Cost)

Using 0.18 um CMOS

2 times/year

(2.5m +1.5m) * 2 =8 M Yen
Approximately US$ 80,000

CAD Tools

Design Tools:

Schematic Design

- Agilent-ADS
- Agilent-Momentum, EMDS (EM software)
- Cadence-Spectre, spice etc

Layout Design

- Cadence-Assura, Virtuso

EM Simulation:
Ansoft: HFSS, FDTD (3D)

MATLAB (with SimuLink)

Fixed Cost Estimation (Additional**) (CAD Tools)

Cost per Unit License (¥)

Agilent Tools: 8 M

Cadence Tools: 9 M

EM Tools: 4 M

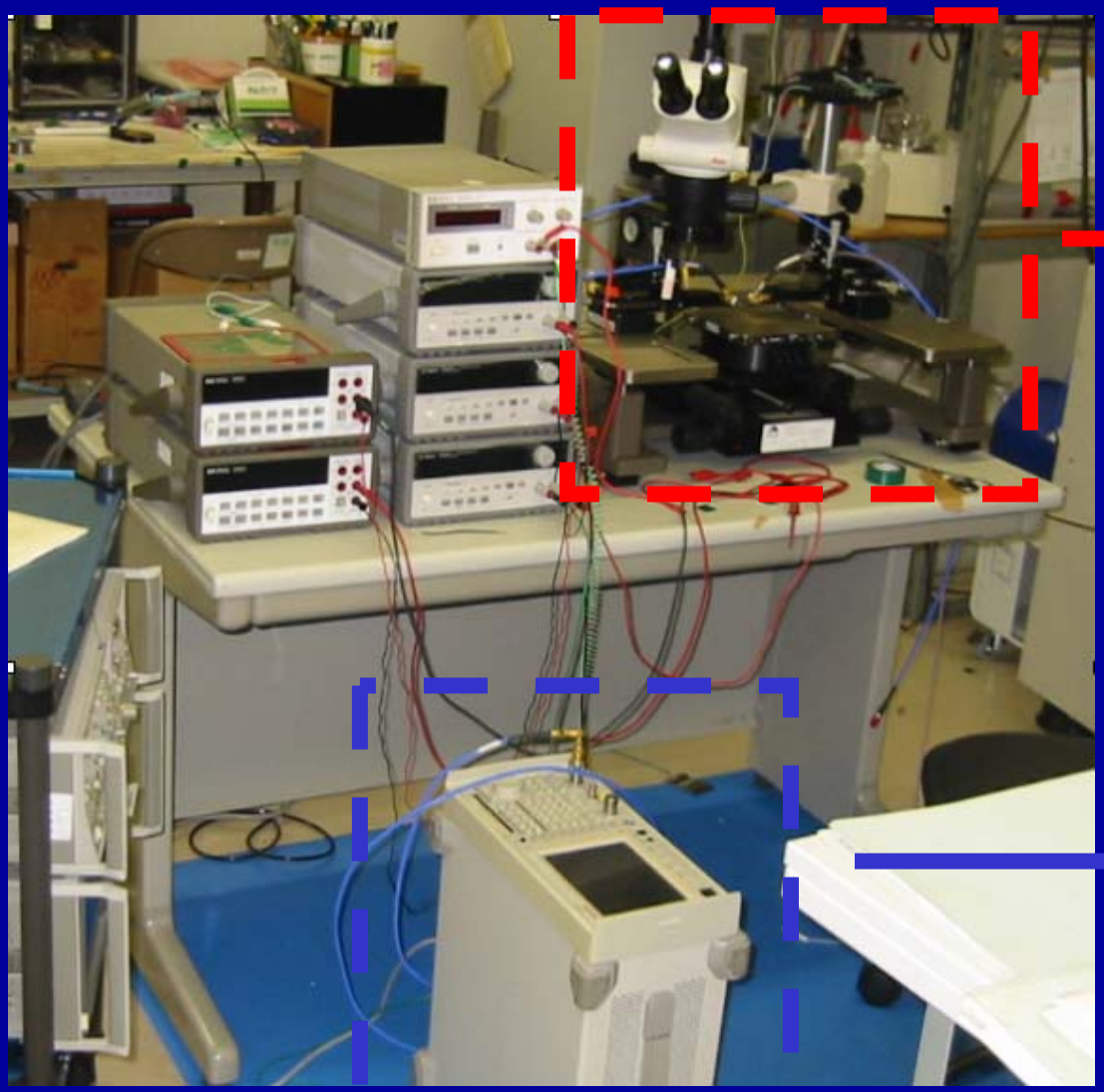
MATLAB: 1 M

Additional Cost/license : 22 M

At least 3 license, additional total cost : 66 M = US$660,000

Additional** does not include the cost for those tools in the list provided by E-JUST officers.

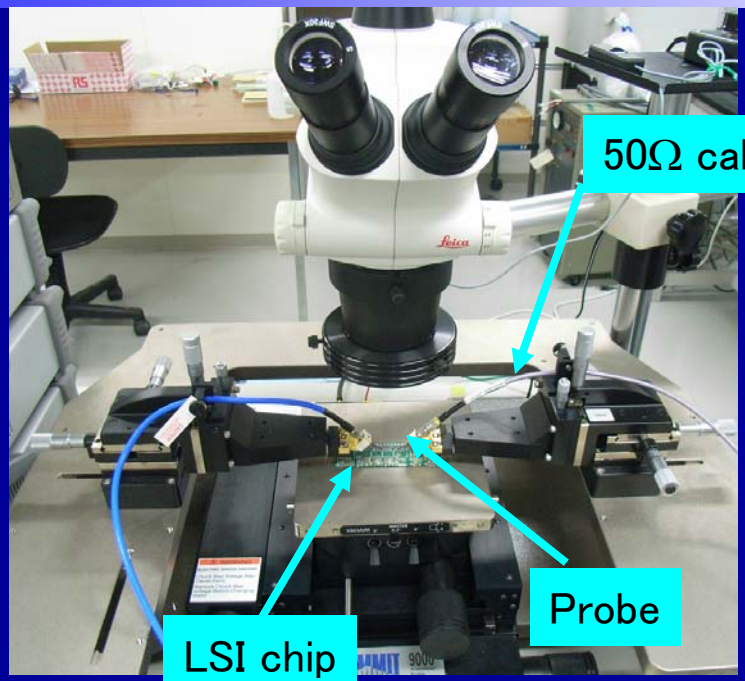
Lab Facilities of Testing



Probe Station

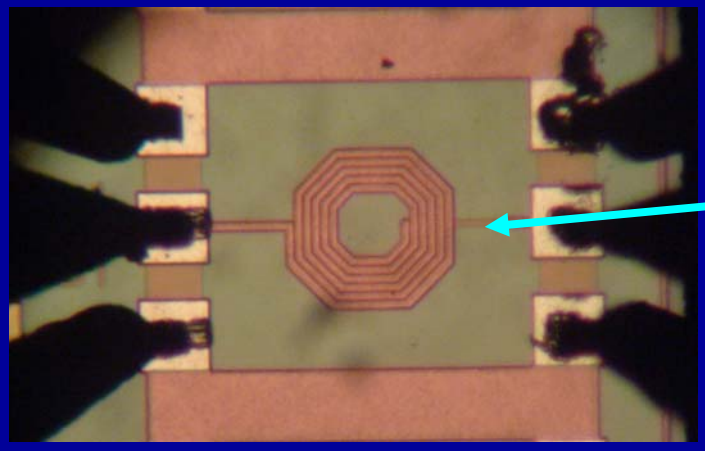
Spectrum Analyzer

Lab Facilities of Testing



Cascade Microtech

Air Coplanar Probe



Spiral inductor

Additional Cost for Equipments (Fixed Cost)

Cost per Unit License (¥)

Probe station: 10 M

Noise Figure Meter: 5 M

Source Signal Analyzer: 11 M

Extra for DC source, probes etc: 2 M

Total = 28 M = US$ 280,000

Additional** does not include the cost for those equipments in the list provided by E-JUST officers.

Total Cost Estimation

Fixed cost (Additional CAD tools) = US$ 660,000

Fixed cost (Additional Equipments) = US$ 280,000

Fixed cost (Fixed Cost provided by E-JUST officers) =US$ **554,748**

Total Fixed Costs = US$1,494,748

Material cost (Chip Fabrication)/year (Using 0.18 um CMOS) = US$ 80,000

Overhead Cost/year = US$20,000

Total Costs = US$1,794,848 for first year.

Digital Laboratory Setup (I)

EDA TOOLS:

Application	EDA Tools
High Level	CyberWorkBench, Comet,
Front-End	VCS, NC-Verilog, VCX MX, Riveira-Pro, Composer IF, Analog HSPICE IF etc
Pre-layout	Design Analyzer, DC ultra, HDL compiler, DFT compiler, power compiler, VHDL compiler
Backend	IC compiler, Calibre, Cadence link, IC compiler

Cost: Approximately US$ 593,445

Digital Laboratory Setup (II)

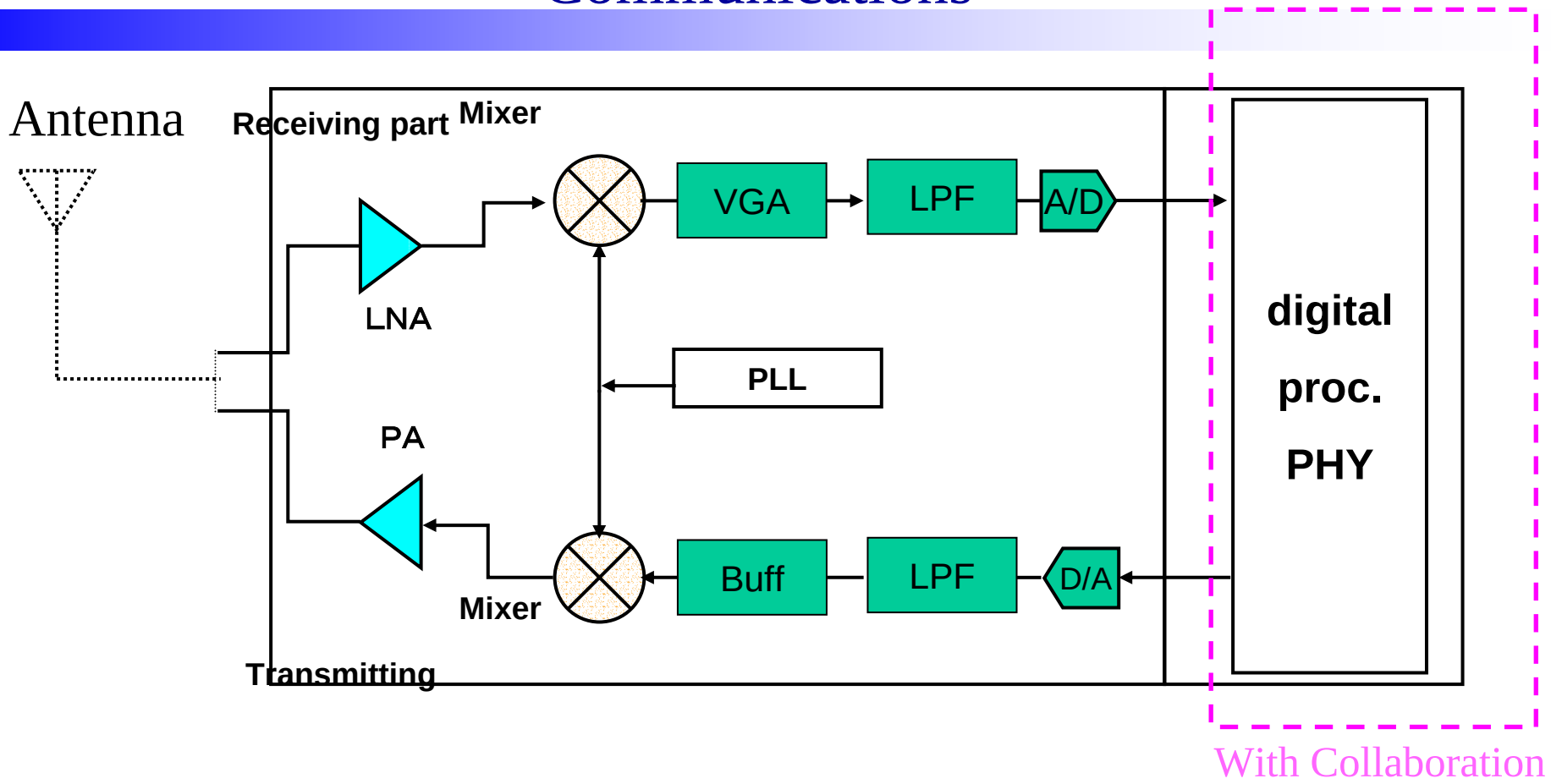
Test Equipments:

LSI Tester	LSI Testers (512 pin, 256 pin, WS only etc)
Other Equipments	Parameter Analyzer, Signal Generator, Laser pair equipments, Signal analyzer, network analyzer, Oscilloscope, Logic analyzer, data generator, digital multimeter, dc sources etc.

Cost: Approximately US$ 900,000

Total cost for Digital Lab setup= US$ 1,493,445

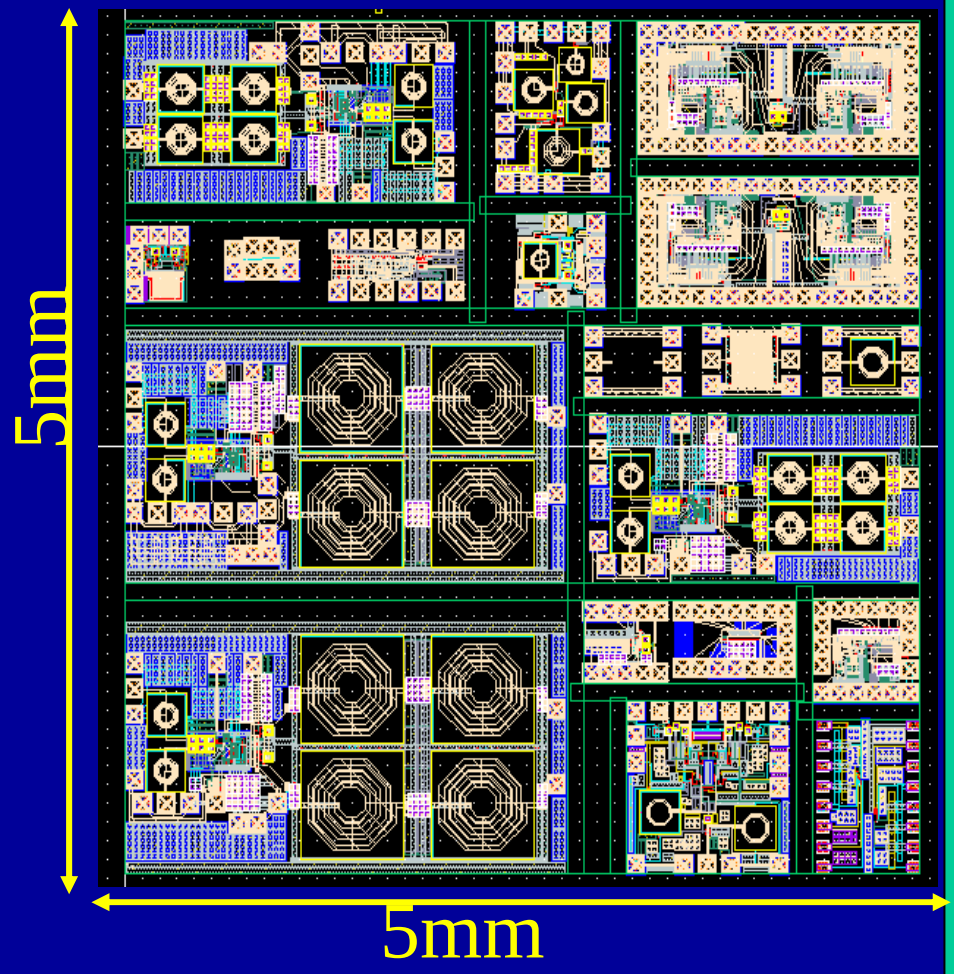
Block diagram of CMOS-LSI System for Wireless Communications



Direct Conversion Receiver Type

1-Chip:SoC Implementation (System on Chip)

Prototype Design [Part-II]



Ultra-wide band (UWB) systems

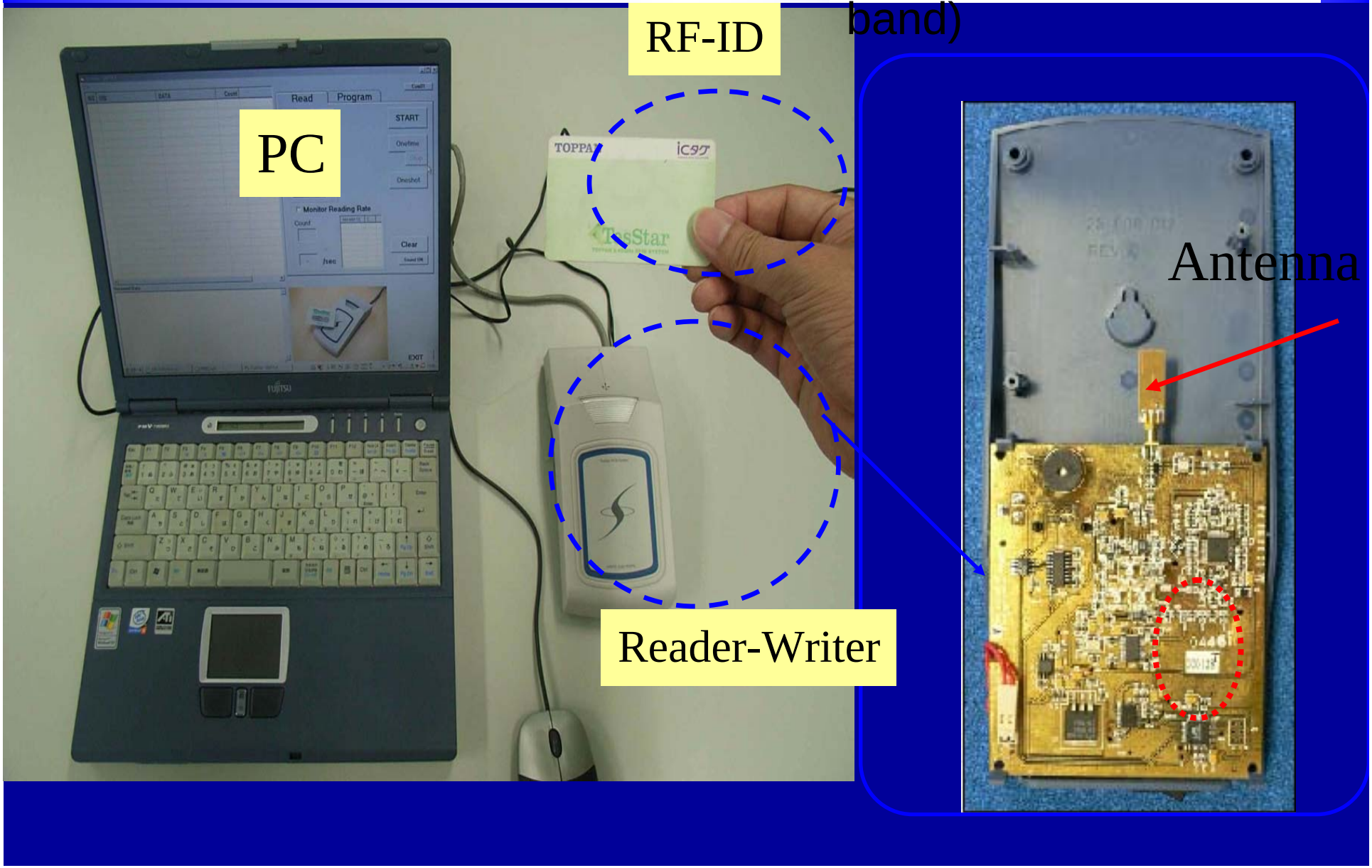
- LNA, mixer, ADC, DAC

For MIMO-MESH Project

- Mixer, VCOs, 1-bit ADC
- Test chips.

Measuring system of communication distance

@2.45GHz (IMS band)



MIMO System: Originality and Dominancy

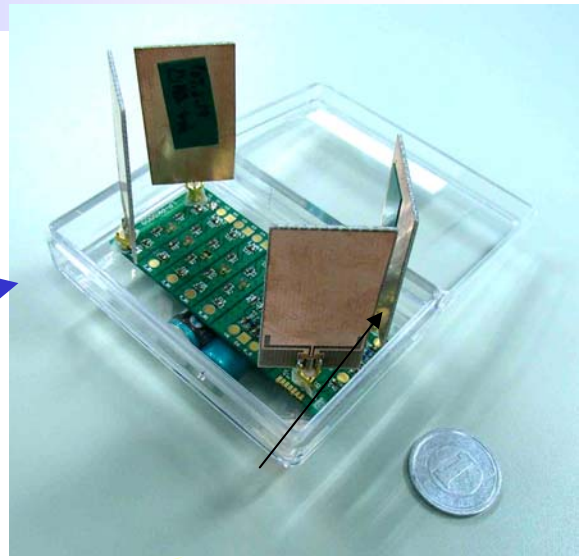
MIMO-MESH. Pico-MESH

Conventional MESH Device

More than 10kg
Limitation= 2~3 hubs

MESH Point

Device Image



RF front end + IP Core

Conclusion

- Microwave Circuits-Filters, Antenna etc.
- RF and Analog Integrated Circuits (RFIC)

Applications:
For MIMO,PICO and UWB

Detail:

Thank you for you kind Attention!