

Electrically Small Antennas with Miniaturized Impedance Matching Circuits for Semiconductor Amplifiers

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SUMMARY In order to reduce the size of a wireless system, we propose a design theory for the broadband impedance matching circuit which connects an electrically small antenna (ESA) to a semiconductor amplifier. We confirmed its validity for the case of connection between a small slot loop antenna with a small radiation resistance of $R_a = 0.776 \Omega$ and a semiconductor amplifier with high input impedance of $Z_L = 321 - j871 \Omega$ with the aid of the simulations by the electrical circuits using transmission lines as well as the electromagnetic field (EM field) simulator. We also made experiments on this antenna with matching circuits using high temperature superconductor YBCO thin films on MgO substrates.

key words: RF front-end, miniaturized matching circuit, electrically small antenna, semiconductor amplifier, coplanar waveguide

1. Introduction

In recent years, the miniaturization of antennas is essential in radio communication devices such as wireless LAN, RF-ID and MIMO since the size of the antenna often determines the whole size of the wireless system [1]–[3]. Studies are also made of an electrically small antenna (ESA), i.e., the antenna whose dimension is much smaller than a wavelength, towards further reduction of the antenna size [4]. It is widely known, however, that in order to realize the miniaturized antenna we must simultaneously realize a broadband impedance matching circuit which compensates the narrow bandwidth peculiar to the small antenna with low radiation resistance [5]–[8], and that we must also attain large impedance-matching ratios to connect with semiconductor amplifiers with high internal impedances.

In this paper we propose a general design theory for the broadband impedance matching circuit which connects a small antenna to a semiconductor amplifier. It is shown that the proposed matching circuits have performances similar to those of the n -pole bandpass filter (BPF) [9]. By using the quarter wavelength transmission line and L-type J -inverter, we can reduce the total antenna size more than the previous works. Theoretical performances of the slot loop antenna with the impedance matching circuit which is designed by the present theory are studied by the electrical circuits using transmission lines (Transmission Line Model) as well as the EM field simulator. In order to demonstrate the theory, we also carried out experiments on the rectangular slot

loop antenna, which has the area of $4 \text{ mm} \times 4 \text{ mm}$, with the prototype matching circuits with pole numbers of $n = 1$ and $n = 2$ using high temperature superconductors YBCO on $15 \text{ mm} \times 15 \text{ mm}$ MgO substrates in the 2.4 GHz band.

2. Design Formulas for Impedance Matching Circuits between ESA and Semiconductor Amplifiers

Figure 1 shows the block diagram of the RF front-end of a typical wireless system, which consists of an antenna, a diode switch, semiconductor amplifiers, i.e., a low noise amplifier (LNA) and a power amplifier (PA), and bandpass filters (BPF) between them, where impedance matching must be attained between the antenna and amplifiers via BPF.

The present design formulas for the impedance matching are derived from the conventional design theory for n -pole Chebyshev BPF consisting of parallel resonators and J -inverters [9], and it acts as impedance matching circuit as well as BPF.

In Figs. 2(a) and 2(b), we show equivalent circuits of the proposed matching circuits, corresponding to the cases of $n = 1$ and $n \geq 2$, respectively. In order to miniaturize the matching circuit we connect the quarter-wavelength impedance transformer with ESA which has low internal impedance Z_a , and we directly connect L-type J -inverter to LNA or PA with high input or output impedance. In the present design theory, we employed only J -inverters, instead of using K -inverters, to avoid the degradation of performances resulting from losses in inverters.

2.1 Matching Circuit with $n = 1$

Figure 2(a) shows the equivalent circuit for the smallest matching circuit, corresponding to BPF with $n = 1$. In this figure, Z_a denotes the internal impedance of ESA and Y_L

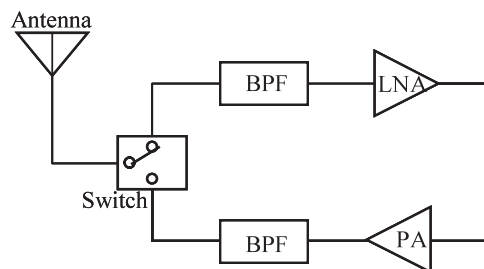


Fig. 1 Block diagram of RF front-end of a typical wireless system.

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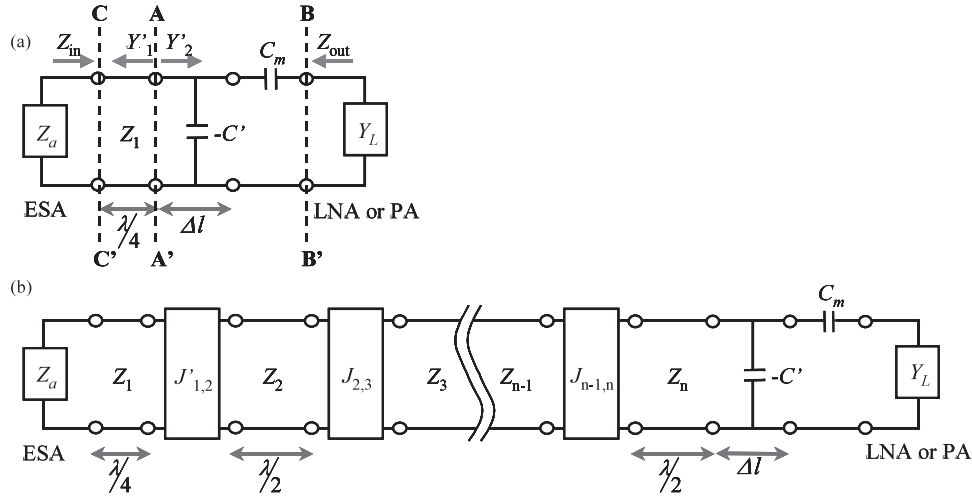


Fig. 2 Impedance matching circuits between ESA and LNA or PA, which have characteristics of BPF in the cases of $n = 1$ (a) and $n \geq 2$ (b).

represents the input admittance of LNA or the output admittance of PA, which are assumed to be given by,

$$Z_a = R_a + jX_a, \quad (1)$$

$$Y_L = G_L + jB_L, \quad (2)$$

where R_a represents radiation resistance and X_a is the reactance of the antenna, which is assumed to be in series resonance in the vicinity of the resonant frequency ω_0 , i.e.,

$$X_a = x_a \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right), \quad (3)$$

with,

$$x_a = \frac{\omega_0}{2} \frac{\partial X_a}{\partial \omega} \bigg|_{\omega=\omega_0}, \quad (4)$$

where x_a is the reactance slope parameter. In Fig. 2(a), Z_1 is the characteristic impedance of the quarter-wavelength resonator, C_m is the coupling capacitor and $-C'$ denotes the virtual capacitor with negative value of capacitance, which can be approximately realized by contraction of the length of an open-ended resonator [5], [9]. The two capacitors C_m and $-C'$ act as L-type J -inverter.

In the case that the antenna impedance is sufficiently low, i.e., $|Z_a| \ll Z_0 (= 50 \Omega)$, which is often the case of ESA, it is shown that the input admittance Y'_1 seen from the right side of the port A-A' is represented near $\omega = \omega_0$ by,

$$Y'_1 = \frac{Z_a}{Z_1^2} + jb_1 \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right), \quad (5)$$

with,

$$b_1 = \frac{\pi}{4} \frac{1}{Z_1}, \quad (6)$$

where b_1 is the susceptance slope parameter of the quarter-wavelength resonator [5], [9]. The characteristic impedance Z_1 must be determined to set the external quality factor (Q)

to a design value:

$$\frac{b_1 + x_a/Z_1^2}{R_a/Z_1^2} = Q_{e1}, \quad (7)$$

$$Q_{e1} = \frac{g_0 g_1}{w}, \quad (8)$$

where Q_{e1} is the design value of the external Q of the input port, g_0 and g_1 are the normalized filter elements, w is the normalized bandwidth [9].

Equations (6) and (7) give the expression for the design value of Z_1 :

$$Z_1 = \frac{4}{\pi} R_a (Q_{e1} - Q_a), \quad (9)$$

with,

$$Q_a = \frac{x_a}{R_a}, \quad (10)$$

where Q_a represents the unloaded Q of the antenna.

The input admittance Y'_2 seen from the left side of the port A-A' is given by,

$$Y'_2 = -j\omega C' + \frac{1}{\frac{1}{j\omega C_m} + \frac{1}{Y_L}}. \quad (11)$$

The values for capacitors C_m and $-C'$ can be determined from another condition for the external Q at the output port at $\omega = \omega_0$:

$$\frac{b_1 + x_a/Z_1^2}{Y'_2|_{\omega=\omega_0}} = Q_{e2}, \quad (12)$$

with,

$$Q_{e2} = \frac{g_1 g_2}{w}, \quad (13)$$

where Q_{e2} is the design value for the external Q of the output

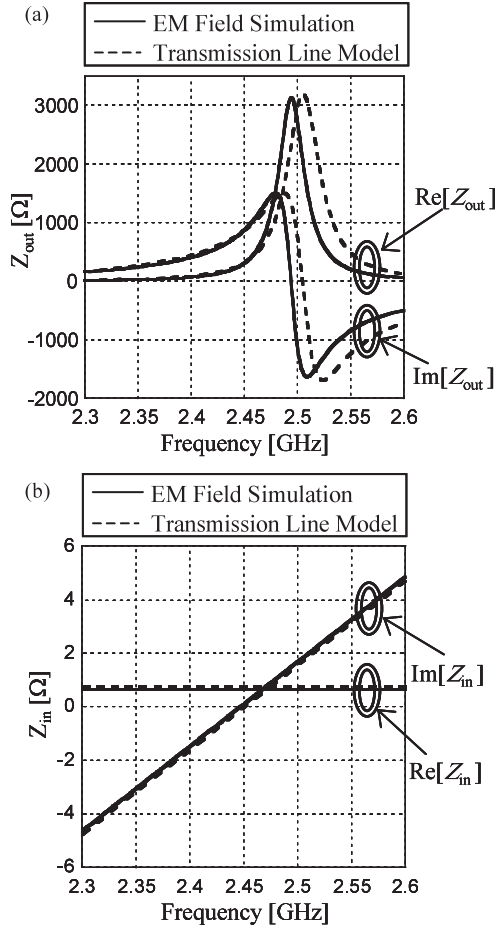


Fig. 3 Frequency dependence of the output impedance Z_{out} (a) and input impedance Z_{in} (b).

end.

Equations (11) and (12) give the expressions for C_m and $-C'$ as,

$$\omega_0 C_m = \frac{G_L}{1 - \gamma_1} \left(\beta \gamma_1 + \sqrt{\gamma_1 (1 + \beta^2 - \gamma_1)} \right), \quad (14)$$

$$-C' = -\frac{C_m (G_L^2 + B_L^2 + \omega_0 C_m B_L)}{G_L^2 + (B_L + \omega_0 C_m)^2}, \quad (15)$$

with,

$$\beta = \frac{B_L}{G_L}, \quad (16)$$

$$\gamma_1 = \frac{b'_1}{G_L Q_{e2}}, \quad (17)$$

$$b'_1 = b_1 + \frac{x_a}{Z_1^2} = \frac{b_1}{1 - Q_a/Q_{e1}}. \quad (18)$$

It is noted that the capacitor with negative value $-C'$ [F] can be realized by the contraction of the length of the open ended portion of the quarter-wavelength resonator by

$$\Delta l = -\frac{C'}{C} [\text{m}], \quad (19)$$

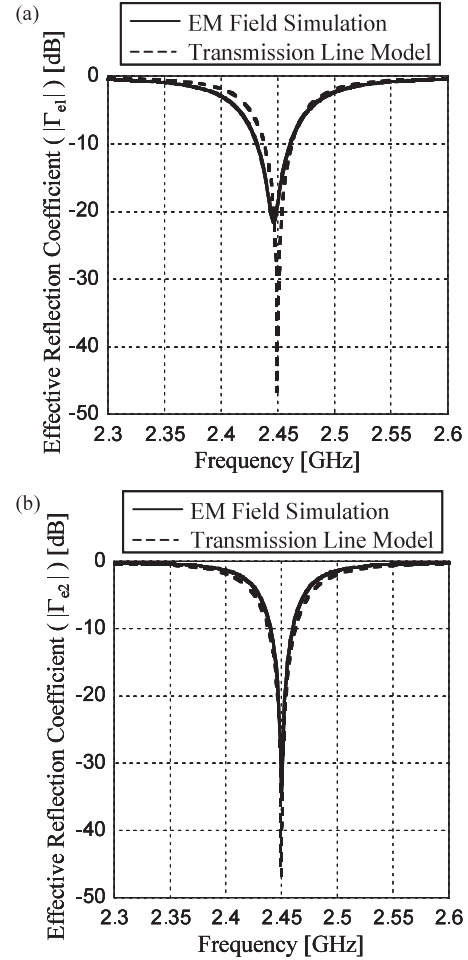


Fig. 4 Frequency dependences of the effective reflection coefficients Γ_{e1} (a) and Γ_{e2} (b).

where C [F/m] is the capacitance of the transmission line per unit length. It must be mentioned that from Eqs. (18) and (25) the applicable range of the present theory is limited to the case of $Q_a < Q_{e1}$, $\gamma < 1$, and also that Q of the transmission line resonator must be larger than Q_{e1} in order to avoid performance degradation.

In Figs. 3(a) and 3(b), we compare the theoretical values of output impedance Z_{out} seen at port B-B' and input impedance seen at port C-C', which were calculated by using the obtained design formulas (Transmission Line Model) and EM field simulator (Agilent: Momentum). In the calculations with transmission line model, we assumed the following values: $f_0 = \omega_0/2\pi = 2.45$ GHz, $w = 3\%$, $Z_1 = 50.6 \Omega$, $R_a = 0.776 \Omega$, $x_a = 13.9 \Omega$, $Y_L = 0.373 + j1.01$ mS, corresponding to $Z_L = 1/Y_L = 321 - j871 \Omega$ [7]. A good agreement was obtained between the two results.

Figures 4(a) and 4(b) show the effective reflection coefficients Γ_{e1} and Γ_{e2} seen at port C-C' and port B-B', respectively, where Γ_{e1} and Γ_{e2} express the degree of impedance matching between a signal source and a load. They are defined by [9],

$$\Gamma_{e1} = \frac{Z_{in} - Z_a^*}{Z_{in} + Z_a}, \quad (20)$$

$$\Gamma_{e2} = \frac{Z_{out} - Z_L^*}{Z_{out} + Z_L}. \quad (21)$$

In the figures, both the results by EM simulation and those by transmission line model are plotted. The good agreement between the two indicates the validity of the proposed design formulas.

2.2 Matching Circuits with $n \geq 2$

The equivalent circuit for the n -pole matching circuit ($n \geq 2$) is shown in Fig. 2. The design formulas can be similarly obtained as,

$$Z_1 = \frac{4}{\pi} R_a (Q_{e1} - Q_a), \quad (22)$$

$$J'_{1,2} = w \sqrt{\frac{b'_1 b_2}{g_1 g_2}}, \quad (23)$$

$$J_{i,i+1} = w \sqrt{\frac{b_i b_{i+1}}{g_i g_{i+1}}} \quad (i = 2, 3, 4, \dots, n-1), \quad (24)$$

$$\omega_0 C_m = \frac{G_L}{1 - \gamma_n} \left(\beta \gamma_n + \sqrt{\gamma_n (1 + \beta^2 - \gamma_n)} \right), \quad (25)$$

$$-C' = -\frac{C_m (G_L^2 + B_L^2 + \omega_0 C_m B_L)}{G_L^2 + (B_L + \omega_0 C_m)^2}, \quad (26)$$

with,

$$b_i = \frac{\pi}{2Z_i} \quad (i = 2, 3, 4, \dots, n), \quad (27)$$

$$\gamma_n = \frac{b_n}{G_L Q_{e2}}, \quad (28)$$

$$Q_{e2} = \frac{g_n g_{n+1}}{w}, \quad (29)$$

where Z_i ($i = 1, 2, 3, \dots, n$) is a characteristic impedance of the transmission line, and b'_1 is given by Eq. (18).

The obtained formulas for the impedance matching circuit are shown to simulate the frequency characteristics of the n -pole BPF [9], where the normalized bandwidth w can be designed for a given pass-band insertion loss ripple, i.e., the minimum return loss in the pass-band. This means that the bandwidth of ESA can be increased by using devices with $n \geq 2$.

3. Design of ESA

3.1 Slot Loop Antenna

The structure of the proposed electrically small slot loop antenna is shown Fig. 5. The total length of the slot loop including feed line is half-wavelength. However, by expanding the length of the feed line we can considerably reduce the area of the antenna, leading to ESA. The backend of the loop is the voltage short-end, thereby the whole operates as

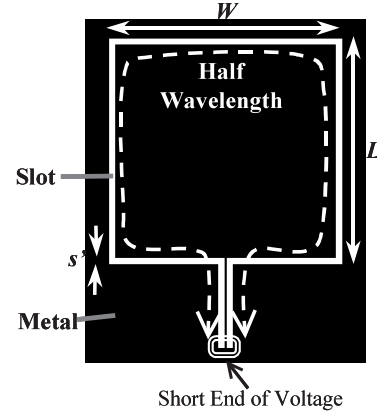


Fig. 5 Layout of slot loop antenna.

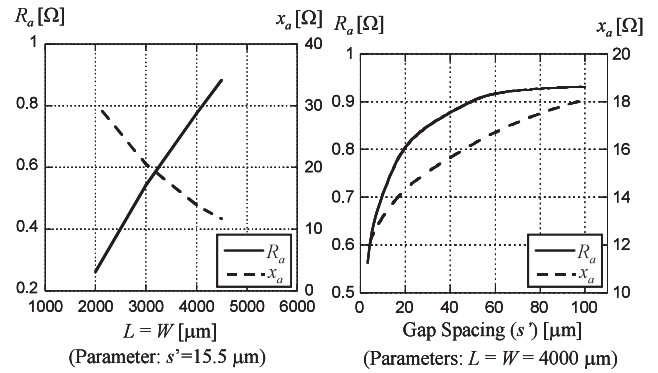


Fig. 6 Loop size dependence of R_a and x_a .

an in-series resonator.

As shown in Fig. 6, the radiation resistance (R_a) and the reactance slope parameter (x_a) of the slot loop antenna are dependent on both the area of the loop and the slot width. In order to realize ESA, the value of L ($= W$) is set to be 4.0 mm. Since a wavelength is about $\lambda = 59$ mm in this case, the total length of the portion of the antenna, that contributes radiation, is reduced to 0.32λ . The frequency dependence of the input impedance of the slot loop antenna (Z_a) is shown in Fig. 7. Thereby, $R_a = 0.776 \Omega$ and $x_a = 13.9 \Omega$ are obtained for the gap spacing $s' = 15.5 \mu\text{m}$.

3.2 Slot Loop Antenna with Matching Circuits

Figures 8(a) and 8(b) show the EM field simulation layouts of the slot loop antennas and matching circuits with pole numbers of $n = 1$ and $n = 2$, respectively. Their design values are $f_0 = \omega_0/2\pi = 2.45$ GHz, $R_a = 0.776 \Omega$, $x_a = 13.9 \Omega$ and $Z_L = Z_0 = 50 \Omega$. In the case of $n = 1$, the designed return loss (RL) and bandwidth (w) are -3 dB and 4%, respectively. On the other hand, in the case of $n = 2$, RL and w are -10 dB and 3%, respectively. The 1-pole matching circuit has a quarter-wavelength transmission line and a J -inverter, and the 2-pole matching circuit has a quarter-wavelength, a half-wavelength transmission line resonator and two J -inverters. J -inverters consist of interdigital gaps,

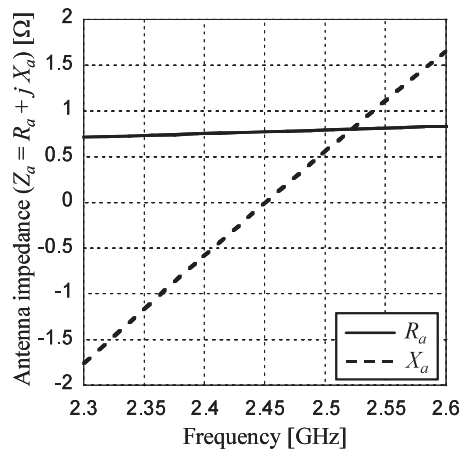


Fig. 7 Antenna impedance of the slot loop antenna (parameters: $L = W = 4.0$ mm, $s' = 15.5$ μ m).

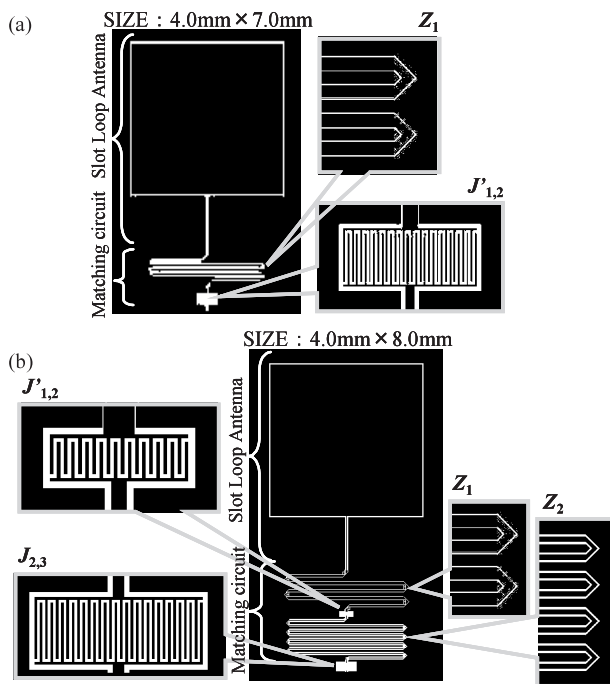


Fig. 8 Layouts and design values of the slot loop antenna with matching circuits in the cases of $n = 1$, return loss (RL) = -3 dB, $w = 4\%$ (a) and $n = 2$, RL = -10 dB, $w = 3\%$ (b).

and in-series resonators consist of meandering CPW. Due to meandering CPW the total size is kept small even if the number of poles increases.

Figures 9(a) and 9(b) show the frequency dependences of return loss which were calculated by EM field simulator in the cases of $n = 1$ and $n = 2$, respectively. These results of simulation are in full agreement with transmission line model results. The desirable bandwidths are obtained, and good impedance matches with feed line are attained in the pass-bands. It is noted that we attained large impedance matching ratio of $Z_0/R_a = 64$ in this case.

In Fig. 10, the normalized radiation pattern at 2.45 GHz

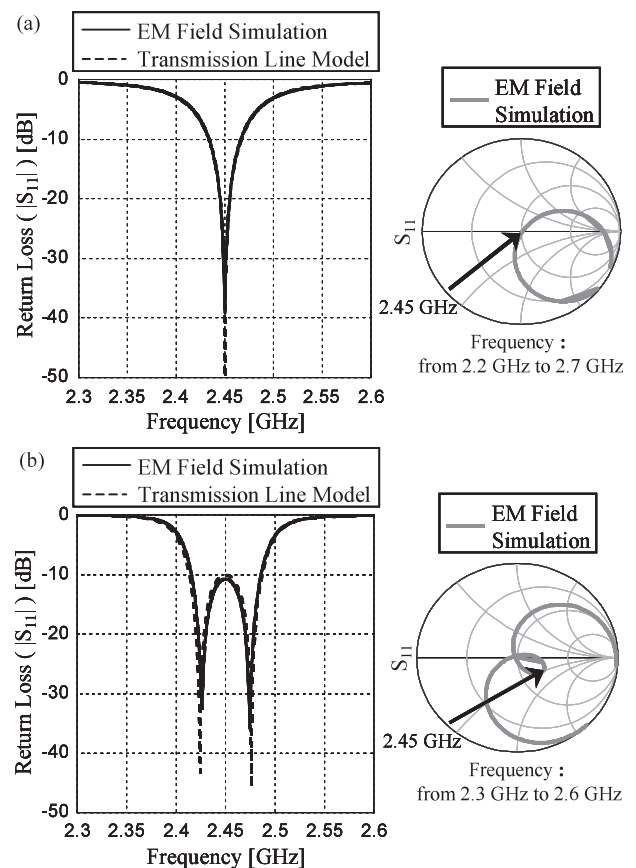


Fig. 9 Simulation results of the frequency dependences of return loss in the cases of $n = 1$ (a) and $n = 2$ (b).

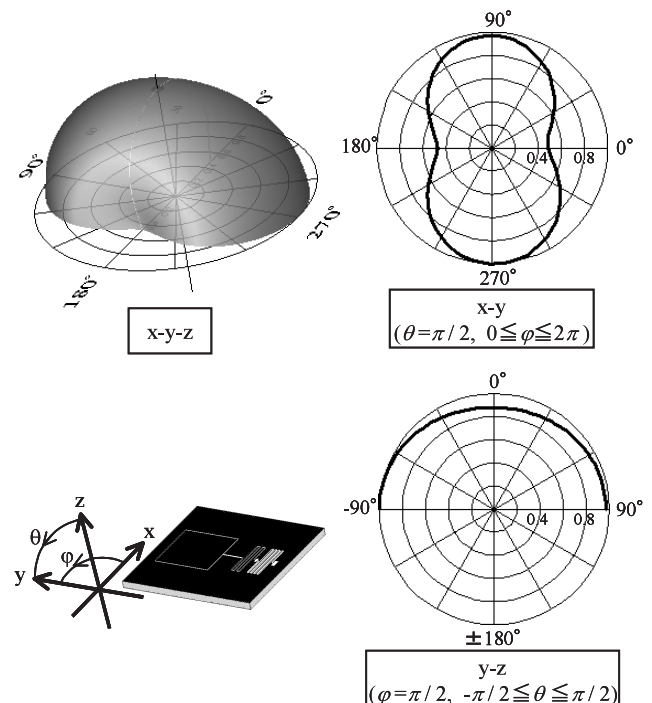


Fig. 10 Directivity pattern of the slot loop antenna.

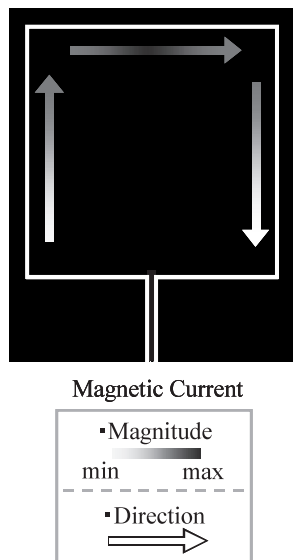


Fig. 11 Magnetic current of the slot loop antenna.

in the case of $n = 2$ is shown. This directivity pattern looks like that of a dipole antenna, since the maximum magnetic current at the backend of a loop portion mainly radiates (see Fig. 11). The same result was also obtained in the case of $n = 1$.

4. Experimental Results

In order to demonstrate the validity of the present theory, we fabricated the slot loop antennas with matching circuits shown in Figs. 8(a) and 8(b) using high temperature superconductor YBCO thin films on MgO substrates whose size is $15 \text{ mm} \times 15 \text{ mm}$. The patterning of the device structure was made by wet etching process and experiments were carried out in a vacuum chamber with refrigerator cooling system.

Figures 12(a) and 12(b) show the experimental results of S -parameter that were measured with vector network analyzer (HP-8722C) by using CPW probes. In the figures, the results of the transmission line model are also plotted for discussion. It must be mentioned that the calculated results were obtained by Eqs. (14) and (15) with $G_L = 1/50 \text{ S}$, $B_L = 0 \text{ S}$, corresponding to $Z_L = 50 \Omega$, and also that we neglected the conductor loss in the simulations. In the case of $n = 1$ (Fig. 12(a)) return loss is reduced to -28.9 dB at 2.37 GHz and impedance matching is achieved. Where, in the case of $n = 2$ (Fig. 12(b)) desirable fractional bandwidth and two peaks that are characteristic of 2-pole filter are observed. The experimental results are not fully in agreement with the simulation result due to the over-etching and the residual loss from the connection of the probe. As shown in Figs. 12(a) and 12(b), the observed center frequencies are shifted to the lower frequency. Their cause seems to be the influence of the kinetic inductance of superconductors [6], [7]. In Figs. 12(a) and 12(b), we added theoretical curves taking account of the apparent increase of the transmission

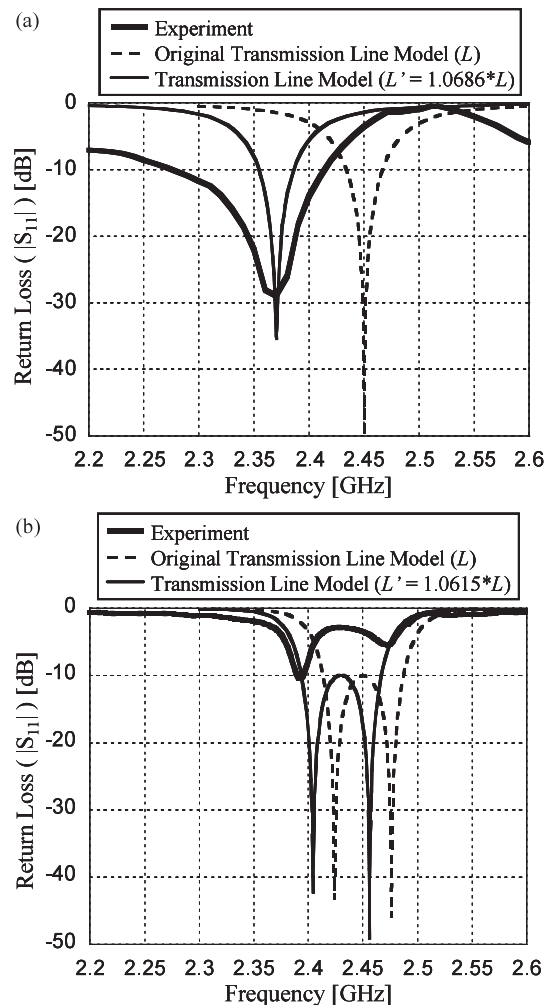


Fig. 12 Experimental results of the frequency dependences of return loss in the cases of $n = 1$ (a) and $n = 2$ (b).

line inductance L due to the kinetic inductance of superconductors.

5. Conclusion

We proposed a design theory for the broadband impedance matching circuit that directly connects a small antenna to a semiconductor amplifier and demonstrated its validity by both simulation and experiment. The impedance of the electrically small slot loop antenna of $R_a = 0.776 \Omega$ was matched to that of a semiconductor amplifier of $Z_L = 321 - j871 \Omega$ by using proposed design formulas. We also fabricated and tested the YBCO slot loop antennas connected to matching circuits with pole number of both $n = 1$ and $n = 2$.

The implementation of the proposed miniaturized antenna onto Si substrate aiming at LSI applications is in progress.

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References

- [1] K. Li, C.H. Cheng, K.F. Tong, T. Matsui, and M. Izutsu, "Millimeter-wave coplanar patch and array antennas," *Proc. APMC 2002*, pp.833–836, Nov. 2002.
- [2] S.C. Gao, L.W. Li, M.S. Leong, and T.S. Yeo, "Dual-polarized slot-coupled planar antenna with wide bandwidth," *IEEE Trans. Antennas Propag.*, vol.51, no.3, pp.421–429, March 2003.
- [3] M.S.A. Salameh, Y.M.M. Antar, and G. Seguin, "Coplanar-waveguide-fed slot-coupled rectangular dielectric resonator antenna," *IEEE Trans. Antennas Propag.*, vol.50, no.10, pp.1415–1419, Oct. 2002.
- [4] R. Azadegan and K. Sarabandi, "A novel approach for miniaturization of slot antennas," *IEEE Trans. Antennas Propag.*, vol.51, no.3, pp.421–429, March 2003.
- [5] K. Yoshida, T. Takahashi, H. Kanaya, T. Uchiyama, and Z. Wang, "Superconducting slot antenna with broadband impedance matching circuit," *IEEE Trans. Appl. Supercond.*, vol.11, no.1, pp.103–106, March 2001.
- [6] H. Kanaya, Y. Koga, J. Fujiyama, G. Urakawa, and K. Yoshida, "Design and performance of high T_c superconducting coplanar waveguide matching circuit for RF-CMOS LNA," *IEICE Trans. Electron.*, vol.E86-C, no.1, pp.37–41, Jan. 2003.
- [7] H. Kanaya, Y. Koga, G. Urakawa, and K. Yoshida, "Design of HTS coplanar waveguide matching circuit for low noise CMOS-HTS receiver," *IEEE Trans. Appl. Supercond.*, vol.13, no.2, pp.1031–1034, June 2003.
- [8] H. Kanaya, G. Urakawa, Y. Tsutsumi, T. Nakamura, and K. Yoshida, "High temperature superconducting slot array antenna connected with low noise amplifier," *Proc. Eucas 2003*, pp.2782–2787, 2003.
- [9] G.L. Matthaei, L. Young, and E.M.T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*, Artech House, Norwood, MA, 1980.



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